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(71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventor: LYON, Richard, C.; 1224 Hopkins Gulch, Boulder Creek, CA 95006 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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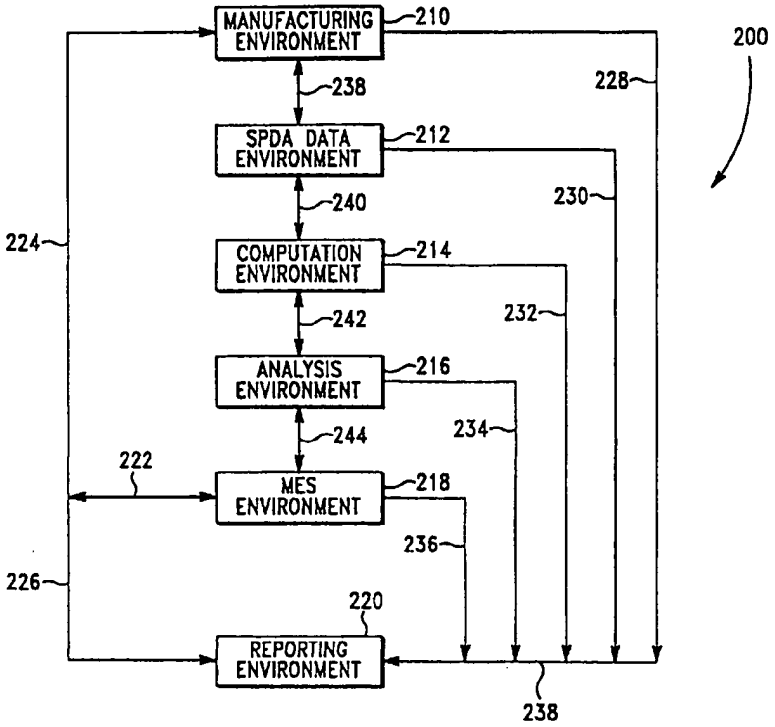
(54) Title: SEMICONDUCTOR PROCESSING TECHNIQUES

(57) Abstract

The present invention provides a manufacturing environment (210) for a wafer fab, and an SPDA data environment (212) for acquiring processing parameters and metrology data of production runs. A computation environment (214) processes the SPDA data to prepare delta graphs (536, 540 and 542) of the present invention. These delta graphs are then analyzed in an analysis environment (216). An MES environment (218) evaluates the analysis and executes a process intervention if the results of the analysis indicate processing or product quality problems in the process run of the manufacturing environment (210). Additionally, the invention provides for SPDA delta graphs of SPC control charts as well as SPC techniques utilizing process control limits based on delta graphs to identify, analyze and trouble-shoot semiconductor processing problems, in order to improve equipment reliability and wafer yield. The present invention also provides a process (700) for computer integrated equipment time states including a service procedures module (755) linked to preventive maintenance time states (735 and 742) and to a repair time state (731).



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SEMICONDUCTOR PROCESSING TECHNIQUES

FIELD OF THE INVENTION

The present invention relates to techniques for semiconductor processing.

BACKGROUND OF THE INVENTION

A semiconductor device such as an IC (integrated circuit) generally has electronic circuit elements such as transistors, diodes and resistors fabricated integrally on a single body of semiconductor material. The various circuit elements are connected through conductive connectors to form a complete circuit which can contain millions of individual circuit elements. Integrated circuits are typically fabricated from semiconductor wafers in a process consisting of a sequence of processing steps. This process, usually referred to as wafer fabrication or wafer fab, includes such operations as oxidation, etch mask preparation, etching, material deposition, planarization and cleaning.

A summary of an aluminum gate PMOS (p-channel metal oxide semiconductor transistor) wafer fab process 40 is schematically shown in FIG. 1, illustrating major processing steps 41 through 73, as described in W.R. Runyan et al., Semiconductor Integrated Circuit Processing Technology, Addison-Wesley Publ. Comp. Inc., p.48, 1994. Each of these major processing steps typically include several sub steps. For example, a major processing step such as metallization to provide an aluminum layer by means of sputter deposition in a wafer fab chamber is disclosed in U.S. Pat. No. 5,108,570 (R.C. Wang, 1992). This sputter deposition process is schematically shown in sub steps 81 through 97 of process 80, see FIG. 2.

FIGS. 1 and 2 show sequential wafer fab processes. It is also known to utilize wafer fab sub systems which provide parallel processing steps. Such sub systems typically include one or more cluster tools. A cluster tool as defined herein includes a system of chambers and wafer handling equipment wherein wafers are processed in the cluster tool chambers without leaving a controlled cluster tool environment such as vacuum. An

example of a cluster tool is disclosed in U.S. Pat. No. 5,236,868 (J. Nulman, 1993) which employs a vacuum apparatus having a central chamber and four processing chambers. A wafer handling robot in the central chamber has access to the interior of each the processing chambers in order to transfer wafers from the central chamber into each of the chambers while keeping the wafers in a vacuum environment. In one example, wafers in the '868 cluster are first transferred for processing to a cleaning chamber, then to a PVD (physical vapor deposition) chamber, followed by transfer to an annealing chamber and subsequently to a degassing chamber, thus utilizing a sequential process. It is also known to use cluster tools such as those disclosed in the '868 patent to process wafers in chambers which are used in parallel. For example, if a slow processing step is followed by a fast processing step, three chambers can be used in parallel for the slow process while the fourth chamber is used for the fast process.

It is well known to those of ordinary skill in the art that one or more processing parameters of a typical wafer fab process step need to be controlled within a relatively narrow range in order to obtain a product which has the desired characteristics. For example, U.S. Pat. No. 5,754,297 (J. Nulman, 1998) discloses a method and apparatus for monitoring a deposition rate during wafer fab metal film deposition such as sputtering. The '297 patent teaches that the metal deposition rate decreases with increasing age of the sputter target if the input sputter power level is maintained at a constant level. As a consequence, critical processing characteristics, such as the metal deposition rate, may vary from run to run for a given wafer fab processing chamber in ways that can affect the yield and quality of devices processed in that chamber. As disclosed in the '297 patent, the deposition system can be more readily maintained near desired levels when processing variables, such as the power input to the sputtering source, are adjusted in response to observed variations in the metal deposition processing characteristics. This requires in-situ measurement of processing characteristics, using for example a deposition rate monitor based on the optical attenuation of light passing through the deposition environment, thereby detecting the rate at which material is flowing from the deposition source to the deposition substrate, as described more fully in the '297 patent.

Advances in semiconductor materials. processing and test techniques have resulted in reducing the overall size of the IC circuit elements, while increasing their number on a single body. This requires a high degree of product and process control for each processing step and for combinations or sequences of processing steps. It is thus necessary to control impurities and particulate contamination in the processing materials such as process gases. Also, it is necessary to control processing parameters such as temperature, pressure, gas flow rates, processing time intervals and input sputter power, as illustrated in the '570 and '297 patents. As illustrated in FIGS. 1 and 2, a wafer fab includes a complex sequence of processing steps wherein the result of any particular processing step typically is highly dependent on one or more preceding processing steps. For example, if there is an error in the overlay or alignment of etch masks for interconnects in adjacent IC layers, the resulting interconnects are not in their proper design location. This can result in interconnects which are packed too closely, forming electrical short defects between these interconnects. It is also well known that two different processing problems can have a cumulative effect. For example, a misalignment of interconnect etch masks which is not extensive enough to result in an electrical short, can still contribute to causing an electrical short if the process is slightly out of specification for allowing (or not detecting) particulate contamination having a particle size which would not have caused an electrical short if the interconnect masks had been in good alignment.

Processing and/or materials defects such as described above generally cause a reduced wafer fab yield, wherein the yield is defined as the percentage of acceptable wafers that are produced in a particular fab. In-process tests and monitoring of processing parameters are utilized to determine whether a given in-process product or process problem or defect indicates that intervention in the process run is necessary, such as making a processing adjustment or aborting the run. Consequently, product and process control techniques are used extensively throughout a wafer fab. When possible, yield problems are traced back to specific product or processing problems or defects to ultimately improve the yield of the wafer fab. High yields are desirable for minimizing manufacturing costs for each processed wafer and to maximize the utilization of resources such as electrical power, chemicals and water, while minimizing scrap re-work or disposal.

It is known to use SPC (statistical process control) and SQC (statistical quality control) methods to determine suitable wafer fab control limits and to maintain the process within these limits, see for example R. Zorich, Handbook Of Quality Integrated Circuit Manufacturing, Academic Press Inc., pp. 464-498, 1991. SPC and SQC methodologies suitable for a wafer fab include the use of control charts, see for example R. Zorich at pp. 475-498. As is well known to those of ordinary skill in the art, a control chart is a graphical display of one or more selected process or product variables, such as chamber pressure, which are sampled over time. The target value of a particular variable and its upper and lower control limits are designated on the chart, using well known statistical sampling and computation methods. The process is deemed out of control when the observed value of the variable, or a statistically derived value such as the average of several observed values, is outside the previously determined control limits. Control limits are typically set at a multiple of the standard deviation of the mean of the target value, such as for example 2σ or 3σ. The target value is derived from a test run or a production run which meets such wafer fab design criteria as yield, process control and product quality. SPC and SQC are considered synonymous when used in the above context, see R. Zorich at p. 464.

Effective wafer inventory management is necessary for maintaining inventories of unprocessed or partly processed wafers at a minimum and thereby minimizing the unit cost of the semiconductor devices which are produced in the wafer fab. Minimizing inventories of wafers in process also has a wafer yield benefit because it is well known that the longer wafers are in the process, the lower their yield. Wafer inventory management typically uses scheduling techniques to maximize equipment capabilities in view of the demand for processed wafers, for example by scheduling parallel and series processing steps to avoid processing bottlenecks. Effective inventory management of a wafer fab also requires a low incidence of bottlenecks or interruptions due to unscheduled down times which can for example be caused by unscheduled maintenance, interruptions resulting from processing parameters which are outside their specified limits, unavailability of required materials such as a process gas, unavailability of necessary

maintenance replacement parts, unavailability of a processing tool such as a chamber, or electrical power interruptions.

Many components or sub-systems of a wafer fab are automated in order to achieve a high degree of processing reliability and reproducibility and to maximize yields. Wafer fab tools such as chambers are typically controlled by a computer using a set of instructions which are generally known as a recipe for operating the process which is executed by the tool. However, it is recognized that a high degree of automation wherein various processes and metrologies are integrated, is difficult to achieve due to the complexity and inter dependency of many of the wafer fab processes, see for example Peter van Zandt, Microchip Fabrication, 3rd ed., McGraw-Hill, pp. 472 – 478, 1997.

It is well known to those of ordinary skill in the art that the functions of semiconductor manufacturing equipment, including for example a wafer fab, can be defined in basic equipment states such as the six states schematically illustrated in FIG. 3, see SEMI E10-96, Standard For Definition And Measurement Of Equipment Reliability, Availability, And Maintainability (RAM), published by Semiconductor Equipment and Materials International (SEMI), pp. 1-23, 1996. The semiconductor industry typically uses these six equipment states to measure and express equipment RAM (reliability availability and maintainability), based on functional equipment issues which are independent of who performs the function. These six basic equipment states include non-scheduled time 102 (FIG. 3), unscheduled downtime 104, scheduled downtime 106, engineering time 108, standby time 110 and productive time 112. Non-scheduled time 102 represents the time period wherein the equipment is not scheduled to be used, for example unworked shift. Unscheduled downtime 104 concerns time periods wherein the equipment is not in a condition to perform its intended function, e.g. during equipment repair. Scheduled downtime 106 occurs when the equipment is capable of performing its function but is not available to do this, such as process setup or preventive maintenance. Engineering time 108 concerns the time period wherein the equipment is operated to conduct engineering tests, for example equipment evaluation. Standby time 110 is a time period wherein the equipment is not operated even though it is in a condition to perform its intended function and is capable of performing its function, for example no operator is available or there is

no input from the relevant information systems. Productive state 112 represents the time period wherein the equipment is performing its intended function, such as regular production and rework.

Total time period 114, see FIG. 3, is the total time during the period being measured; this includes the six equipment states 102, 104, 106, 108, 110 and 112. Operations time 116 concerns the total time period of states 104, 106, 108, 110 and 112. Operations time 116 includes equipment downtime 118 consisting of states 104 and 106, and equipment uptime 120. Equipment uptime 120 includes engineering time 108 and manufacturing time 122 which consists of standby time 110 and productive time 112.

FIGS. 4 and 5 provide more detailed schematic illustrations of the six equipment states shown in FIG. 3, see SEMI E10-96, at pp. 1-6. As depicted in FIG. 4, total time 114 consists of non-scheduled time 102 and operations time 116. Non-scheduled time 102 includes unworked shifts 130, equipment installation, modification, rebuilding or upgrading 132, off-line training 134 and shutdown or start-up time period 136. Operations time 116, as schematically illustrated in FIG. 5, consists of equipment downtime 118 and equipment uptime 120. Equipment downtime 118 consists of unscheduled downtime 104 and scheduled downtime 106. Unscheduled downtime 104 includes downtime for maintenance delay 140, repair time 142, changing consumables/chemicals 144, out of specification input 146 or facilities related downtime 148. Scheduled downtime 106 concerns downtime for maintenance delay 150, production test 152, preventive maintenance 154, changing consumables/chemicals 156, setup 158 or facilities related 159.

Equipment uptime 120, depicted in FIG. 5, consists of engineering time 108 and manufacturing time 122. Engineering time 108 includes process experiments 160 and equipment experiments 162. Manufacturing time 110 consists of standby time 110 and productive time 112. Standby time 110 includes time during which there is no operator 180, no product 182, no support tool 184 or when an associated cluster module is down 186. Productive time 112 concerns a time period during which there is regular production 190, work for a third party 192, rework 194 or an engineering run 196. The various

equipment states as described in connection with FIGS. 3 – 5 provide a basis for communicating and evaluating RAM related equipment information in the semiconductor industry. RAM related equipment information includes topics which are well known to those of ordinary skill in the art such as: equipment reliability, equipment availability, equipment maintainability and equipment utilization, see for example SEMI E10-96 at pp. 6-11.

Accordingly, a need exists for methods and techniques which provide improved process control, quality, yield and cost reduction. Also, there is a need to integrate the equipment time states to provide enhanced process scheduling and improved utilization of processing equipment.

SUMMARY OF THE INVENTION

The present invention provides novel techniques for semiconductor processing, particularly for wafer manufacturing. These novel techniques provide the needed improvements in process control, quality, yield, equipment scheduling and cost reduction.

In one embodiment of the present invention, a novel delta analysis technique is employed to determine if there are significant processing or performance differences between two semiconductor processing runs using the same recipe in a tool such as a wafer fab chamber. Processing parameter or metrology data of the first run are plotted versus time to obtain a graph of data, such as gas flow rate, against time. A similar graph is prepared using data from the second processing run. The graphs are overlayed in a synchronized manner, e.g. the graphs are overlayed such that they start at the same time event, such as process startup. The data of one of the overlayed graphs are subtracted from the data of the other graph thereby forming a novel delta graph. Computer implemented delta graph analysis facilities the identification, analysis and trouble-shooting of semiconductor processing and/or performance problems, such as inconsistencies between processing runs

In another embodiment of the present invention, the same semiconductor processing recipe was used for production runs in two semiconductor processing chambers. Processing parameter or metrology data, such as chamber pressure, from one chamber were plotted versus time resulting in a graph of data versus time. A similar graph was prepared using data versus time from the other chamber. Subsequently, a synchronized graph overlay was prepared of the two graphs. The data of one of the overlayed graphs were subtracted from the data of the other graph, thus forming a delta graph. The delta graph was then used to determine of there were significant processing or performance differences between these chambers, when using this particular recipe. The computer implemented novel delta graph is utilized to identify, analyze or trouble-shoot performance differences between the chambers, thus leading to greater wafer fab processing uniformity, improved equipment utilization and improved wafer yield.

In yet another embodiment of the present invention, a quality control chart is prepared of a semiconductor processing run such as a test run or a standardized run. A quality control chart of a production run is then prepared using the same recipe in the same chamber. A synchronized overlay chart is prepared using the test run control chart and the production run control chart. A computer implemented delta graph is then prepared by subtracting the data of one chart from the other chart. The delta graph is analyzed to determine if there are significant differences between the production run and the test run, thus providing a method for analyzing the production run and improving wafer yield.

In still another embodiment of the present invention, a quality control chart for matching two wafer fab tools is prepared by executing a statistically significant number of process runs in these tools, using the same recipe in both tools. Computer implemented delta graphs are then constructed by plotting the same parameter from each tool versus time and subtracting the data of one tool from the data of the other tool. An analysis is then performed to determine which processing runs resulted in satisfactory tool matching performance. The delta graphs representing these runs are subsequently used to develop

control limits. which can be used to evaluate the chamber matching performance of subsequent process runs.

In another embodiment of the present invention, computer integrated equipment time states are provided to facilitate manual and automatic scheduling of equipment functions and to provide an improved capability to respond to processing conditions. The time states can be enabled by a user through interactions with the computer through which the time states are integrated. In one embodiment of this invention, a service procedures module is provided which is automatically linked to one or more of these equipment time states and which is activated when one of these time states is enabled.

In yet another embodiment of the present invention, computer integrated equipment time states are integrated with the process which is executed in the equipment. Process/quality process control techniques of this process are linked to one or more equipment time states, causing the equipment to go off-line when the process is not operating within predetermined process/quality control limits.

In another embodiment of the present invention, the novel computer integrated time states are adapted to keep track of, and respond to, maintenance trigger events which automatically enable a preventive maintenance time state of a tool upon the occurrence of the trigger event. Examples of maintenance trigger events include a predetermined total wafer count and a predetermined total operating time of a tool.

Other embodiments of the present invention include digitally coded data structures stored in a memory. The data structures include delta graph methodologies and equipment time states of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flowchart schematically illustrating a prior art wafer fab process.

FIG. 2 is a flowchart schematically illustrating a prior art wafer fab sputter metallization process.

FIG. 3 is a stack chart schematically illustrating prior art equipment time states.

FIG. 4 is a block diagram schematically showing prior art equipment time states of the stack chart illustrated in FIG. 3.

FIG. 5 is a block diagram schematically showing prior art equipment time states of the stack chart illustrated in FIG. 3.

FIG. 6 is a block diagram schematically showing a semiconductor process of the present invention.

FIG. 7 is a block diagram schematically showing another semiconductor process of the present invention.

FIG. 8 is a block diagram schematically showing a wafer fab chamber of the process illustrated in FIG. 7.

FIG. 9 is a block diagram schematically showing a computation environment of the process illustrated in FIG. 7.

FIG. 10 is a graphical illustration of chamber bias forward power versus time, of the process illustrated in FIG. 7.

FIG. 11 is a graphical illustration of chamber pressure versus time, of the process illustrated in FIG. 7.

FIG. 12 is a flowchart schematically illustrating a method of constructing a delta graph of the present invention.

FIG. 13 is a graphical illustration of two overlayed graphs of chamber bias forward power versus time, of the process illustrated in FIG. 7.

FIG. 14 is a graphical illustration of a delta graph of bias forward power difference versus time, of the overlayed graphs shown in FIG. 13.

FIG. 15 is a graphical illustration of two overlayed graphs of chamber pressure versus time, of the process shown in FIG. 7.

FIG. 16 is a graphical illustration of a delta graph of chamber pressure difference versus time, of the overlayed graphs shown in FIG. 15.

FIG. 17 is a graphical illustration of a delta graph of chamber RF peak-to-peak voltage difference, of the process shown in FIG. 7.

FIG. 18 is a block diagram schematically showing an additional semiconductor process of the present invention.

FIG. 19 is stack chart schematically showing another embodiment of the present invention.

FIG. 20 is a block diagram schematically illustrating equipment time states of the stack chart illustrated in FIG. 19.

FIG. 21 is a block diagram schematically showing equipment time states of the stack chart illustrated in FIG. 19.

DETAILED DESCRIPTION OF THE INVENTION

While describing the invention and its embodiments, certain terminology will be utilized for the sake of clarity. It is intended that such terminology includes the recited embodiments as well as all equivalents.

One embodiment of the invention, schematically illustrated in FIG. 6, shows a novel semiconductor process 200 employing SPDA (semiconductor process delta analysis) of the present invention. As defined herein, an SPDA includes a semiconductor processing technique wherein two graphical presentations of processing or performance data versus time are synchronized and overlayed. The data of one graph are then subtracted from the data of the other graph, thereby providing a delta graph as will be described more fully in connection with FIGS. 10 - 17. As used herein, SPDA is suitable for analyzing the performance of one specific tool, a combination of several tools, a cluster tool, a wafer fab or several wafer fabs. Novel semiconductor process 200, shown in FIG. 6, includes a manufacturing environment 210, an SPDA data environment 212, a computation environment 214, an analysis environment 216, an MES environment 218 and a reporting environment 220. The expression "environment" as defined herein, includes an aggregate of technologies, methods an/or devices which provide a resource for acquiring data, data structures or information and which, optionally, can interact with the acquired data, data structures or information. An environment as used herein, includes a computer environment. The expression "computer environment" as defined herein, includes computer software and/or hardware which provides a resource for acquiring data, data structures or information and which can interact with the acquired data, data structures or information.

Manufacturing environment 210, depicted in FIG. 6, includes manufacturing apparatus, techniques and methods to manufacture wafer fab devices or device components such as IC structures. The expression "IC structures" as defined herein, includes completely formed ICs and partially formed ICs. The manufacturing environment includes such controllers and inputs as are necessary to form the IC structure. Suitable controllers include processors for example micro processors such as on-board computers, computer operated software and mechanical/electrical controllers such as switches and electrical circuits employing for example a variable resistor such as a potentiometer. These controllers operate or control various processes and operational functions, such as gas flow rate and wafer handling within manufacturing environment 210. Suitable examples of manufacturing environments such as 210 include a wafer fab tool, such as a chamber, a combination of several tools, a cluster tool, or one or more wafer fabs.

SPDA data environment 212, depicted in FIG. 6, is adapted for receiving information from manufacturing environment 210. This information can include processing information and run or wafer ID information. Information such as for example chamber pressure during all or part of a processing run can be collected during specific time intervals using methodologies or techniques such as are well known to those of ordinary skill in the art. Computation environment 214, for example using a data processor, is employed to chart or plot the information collected in SPDA data environment 212. Data, such as chamber pressure data, can be charted versus time for a particular run, or for the processing of a specific wafer. The data collection and charting process can be repeated for several processing runs. Graphs or charts thus obtained can be employed to develop an SPDA by synchronizing the graphs to a common processing event, such as a startup event, and subtracting the pressure data of one graph from the data of the other graph at each of the time intervals of the chart. This subtraction process results in a delta graph wherein the subtraction results are plotted versus time. The term "delta graph" as defined herein includes a graph resulting from the subtraction of one graph from another graph in a synchronized overlay of the graphs, as will be described more fully in connection with FIGS. 10 and 12 - 15. The term "synchronized" as defined

herein includes a charting technique wherein two graphs are overlayed such that they share a common event or datapoint which coincides when the graphs are overlayed. The term "shared event" as defined herein includes an event or datapoint which is common to two or more graphs, such as for example an event wherein time equals zero at the startup of a process wherein data are plotted versus time.

Analysis environment 216, see FIG. 6, is provided to analyze the delta graphs. For example, when two processing runs are identical the resulting delta graph is a substantially straight line which is approximately parallel to the time axis of the graph and wherein each data point on the graph has a value of about zero. Any statistically significant deviation from a substantially straight line indicates that there are differences between the two processing runs, thereby indicating a possible processing and/or equipment problem or malfunction. SPDA thus assists in the identification and trouble-shooting of semiconductor processing techniques and/or equipment performance. While analysis environment 216 is shown as a separate environment, it is also contemplated to incorporate the analysis environment in SPDA data environment 212 or in computation environment 214.

MES (manufacturing execution system) environment 218, shown in FIG. 6, provides the information, control, decision making and coordinating functions of the production related activities of novel semiconductor process 200. MES environment 218 acquires the results of the SPDA analysis as determined in analysis environment 216. The MES environment then determines whether the process of manufacturing environment 210 is within or outside the predefined processing parameters or processing criteria. A decision making function in MES environment 218 can then be invoked to decide whether or not to initiate intervention in manufacturing environment 210. Such intervention can include aborting the run, adjusting parameters such as chamber pressure, scheduling additional wafers for processing or scheduling repair or maintenance activities. This intervention can be executed through links 222 and 224 of process 200, as shown in FIG. 6. Optionally, process 200 is provided with a reporting environment 220 to acquire data and other information from the environments of the present invention, for example using links 228, 230, 232, 234 236 and 238 depicted in FIG. 6. Also, when MES environment

218 is linked to manufacturing environment 210, a report can simultaneously be generated using link 226 to reporting environment 220. The above described links as well as links 238 (FIG. 6), 240, 242 and 244 include hard wire connections, wireless connections and links which are provided by manually communicating data and information between the various environments of process 200. These linking techniques are well known to those of ordinary skill in the art.

FIG. 7 is a schematic illustration of another embodiment of the present invention showing novel semiconductor process 300 employing SPDA of the present invention, employing two wafer processing chambers. Process 300 includes a manufacturing environment 310, comprising wafer processing chambers 312 and 314, an SPDA data environment 320, a computation environment 330, an analysis environment 340, an MES environment 350 and a reporting environment 360. Optionally, the MES environment can also include an MIS (management information system) component (not shown). Preferably, environments 320, 330, 340, 350 and 360 comprise computer environments.

FIG. 8 illustrates wafer processing chamber 312 of novel process 300 which receives various inputs from MES environment 350, for example setting or regulating chamber controllers such as controllers 410, 412, 414, 416, 418 and 420, and providing information to input devices 422 and 424. Based on MES input from MES environment 350, chamber status controller 410 is employed to select the status of the chamber: on-line in standby 426, on-line in process 428 or off-line 430. Controller 412 is utilized to select the chamber status as linked 432 or not linked 434 to a wafer fab system (not shown). Controller 414 controls parameters 436 of the facilities systems, such as electrical power, water and waste product removal. Controller 416 controls chamber processing parameters 438, such as process gas flow rate and pressure. Chamber metrology parameters 440 are controlled by controller 418, these include controlling in-process test parameters such as for example the '297 sputter deposition rate monitor, and test sampling frequency. Wafer handling parameters 442, such as the operational parameters of a wafer handling robot, are controlled by controller 420. Input from MES environment 350 can also be utilized to abort a production run, for example using chamber status controller 410 to put the chamber in an off-line status and thereby stop all processing functions of the chamber.

MES environment 350, see FIGS. 7 and 8, can be utilized to provide production run information 444 by means of production run information input device 422. Such information can include run identification, date or purpose of the run, e.g. testing, production or re-work. Wafer and wafer lot identification 446 in chamber 312 of manufacturing environment 410 can be provided by means of wafer identification input device 424. Chamber metrology results 458 are obtained from the use of test procedures employing chamber metrology parameters 440. These results include for example the rate at which material is flowing from a sputter deposition source to a deposition substrate, as disclosed in the '297 patent, chamber pressure, or gas flow rate. Optionally, chamber 312 can receive additional inputs through non-MES input 355, for example a response to an alarm signal which is generated by a component of chamber 312.

Process 300 of the present invention utilizes an SPDA environment 320, as illustrated in FIG. 7, to acquire data such as in-process metrology results wafer ID or run information from chamber 312 of manufacturing environment 310. SPDA data acquisition from chamber 312 is schematically illustrated in FIGS 7 and. 8 as follows. Production run information 444 and wafer ID 446 data as well as chamber metrology parameter information 440 and metrology results 458 can be provided to SPDA environment 320 through a link 455.

Computation environment 330, depicted in FIGS. 7 and 8, is utilized to perform the calculations to support the data processing and reporting of the SPDA environment, as will be described more fully in connection with FIGS. 10 and 11. As illustrated in FIG. 9, computation environment 330 typically includes a processor such as a microprocessor 510, algorithms or data structures 511, a database 512, a memory 513, a first novel algorithm 514, a second novel algorithm 515, optionally a network component 516 and optionally an AI (artificial intelligence) component 517.

Algorithms or data structures 512 (FIG. 9) are employed using methods which are well known to those of ordinary skill in the art to operate processor 510 and any peripheral devices associated with this processor, as well as for processing such

information as metrology and wafer ID data which are acquired in SPDA environment 320. For example, SPDA environment 320 collected bias forward power versus time of a semiconductor etch process in chamber 312. These data were communicated to computation environment 330 using such data communication techniques as are well known to those of ordinary skill in the art. The data were then computed in the computation environment, using for example algorithms 511, to obtain graph 518, shown in FIG. 10, wherein bias forward (i.e. cathode) power is plotted versus time. Similarly, SPDA environment 320 acquired chamber pressure versus time data of an etch process executed in chamber 312. The data were computed in computation environment 330, resulting in graph 519, depicted in FIG. 11. Algorithms 511 for plotting data such as the results in graphs 518 and 519 are well known to those of ordinary skill in the art. Graphs 518 and 519 can be maintained in computation environment 330 in digital form, or can be displayed on a computer monitor. Additionally, the graphs can be provided in printed form, using for example reporting environment 360, shown in FIG. 7.

Chamber 314, shown in FIG. 7, is similar to chamber 312, depicted in FIGS. 7 and 8. Data from chamber 314 are collected in SPDA environment 320 (FIG. 7) using techniques similar to those described in connection with FIGS. 10 and 11. Using these techniques, SPDA data environment 320 acquired bias forward power versus time data, as well as chamber pressure versus time data for the same etch processes as were used to collect these data from chamber 312. The data obtained from chamber 314 were then plotted to obtain graphs using the techniques which were employed in plotting graphs 518 (FIG. 10) and 519 (FIG. 11) concerning chamber 312. Subsequently, novel algorithm 514 (FIG. 9) was employed to make graph overlays as schematically illustrated in FIG. 12. Bias forward digital transducer signal 522 from chamber 312 and bias forward power digital transducer signal 524 from chamber 314 were synchronized in step 526. The synchronized outputs were then overlayed, see step 528, to construct an overlay of graphs 518, i.e. the bias forward power versus time graph of chamber 312 and graph 534 which is the corresponding graph from chamber 314. The synchronized overlay of graphs 518 and 534 is shown in FIG. 13.

Next, in accordance with the present invention, novel algorithm 515 (FIGS. 9 and 12) was employed to subtract the bias forward power data of graph 518 from those of graph 534 in step 530, shown in FIG. 12. In this step, the digital transducer output of chamber 312 was subtracted from the synchronized digital transducer output of chamber 314. Subsequently, a delta graph was formed in step 532 as a result of the subtraction of the transducer outputs. The resulting delta graph 536 is shown in FIG. 14. Delta graph 536 thus depicts the difference in bias forward power between chambers 312 and 314 during the etching process which was employed. It can be concluded from this graph that there were significant differences in bias forward power between chambers 312 and 314. Surprisingly, a comparison between FIGS. 12 and 13 shows that the performance differences between chamber 312 and 314 are more clearly shown in delta graph 536 (FIG. 14) of the novel SPDA, then they are in the overlay of graphs 518 and 534 (FIG. 13).

The techniques and methods which were used to prepare the graph overlay of graphs 518 and 534 were similarly used to prepare graph overlays of chamber pressure versus time for chambers 312 and 314. As illustrated in FIG. 15, a synchronized overlay was prepared of graph 519 (FIG. 11), i.e. chamber pressure versus time of the etching process of chamber 312, and graph 538 representing chamber pressure versus time of chamber 314. Delta graph 540, see FIG. 16, of the present invention was prepared by subtracting the chamber pressure data of graph 538, i.e. chamber 314, from those of graph 519, i.e. chamber 312. A comparison between the overlay graphs shown in FIG. 15 and the delta graph depicted in FIG. 16 illustrates more clearly that there were pressure performance differences between chambers 312 and 314.

Delta graph 542 shown in FIG. 17, was obtained by employing the SPDA techniques of the present invention. This delta graph is the result of the subtraction of the RF peak-to-peak voltage (i.e. the total voltage drop across a source coil) versus time graphs of two processing chambers similar to chambers 312 and 314 using the same recipe, employing the methods and techniques described in connection with FIGS. 10 – 16. Delta graph 542 shows significant performance differences between the two chambers in regard to the RF peak-to-peak voltage.

Returning to FIG. 9, database 512 of computation environment 330 can contain chamber parameter, metrology and wafer ID or run data. Memory 513 can for example be used to store in-process metrology data. Optional network component 516 provides a link between novel process 300 and external entities such as a remote database or a remote management function using for example a bus or a LAN (local area network). Optional AI component 517 can for example be used to process the data stored in database 512 to select metrology parameters and data, based on experience gained over many production runs. Computation environment 330, as described herein, is utilized in conjunction with SPDA methodologies and procedures of the present invention. However, it is also contemplated to use this computation environment for any and all functions of processes carried out in connection with manufacturing environment 310. Links between the various environments of novel process 300 are schematically illustrated in FIG. 7. These links include hard wire connections, wireless connections and links which are provided by manually communicating data and information between the various environments of process 300. These linking techniques are well to those of ordinary skill in the art.

It is also contemplated to provide a novel product or a novel apparatus comprising one or more digitally coded data structures including novel algorithms 514 and 515 (FIG. 12) stored in a memory. Suitable memories for this novel product include removable electronic data storage devices, such as computer disks, magnetic tapes and optical disks. Suitable memories for a novel apparatus include data processing devices, such as computers, having a memory.

As schematically shown in FIGS. 7 and 9, an analysis environment 340 is provided to analyze the results of the SPDA techniques of the present invention to identify, trouble-shoot or correct processing or equipment problems in IC processing. For example, an analysis of delta graphs 536, 540 and 542 shown in FIGS. 14, 16 and 17 respectively, indicate that there are significant performance differences between chambers 312 and 314 of manufacturing environment 310 depicted in FIG. 7. This means that adjustments need to be made in the processing parameters of one of the chambers, or of both chambers, in order to match chambers. Such chamber matching can be important in

wafer yield enhancement and scrap reduction, as well as reducing the time which is required to ready a wafer fab for production. While analysis environment 340 has been shown as an environment which is separate from the other environments of this invention, it is also contemplated to integrate analysis environment 340 with computation environment 330 (FIG. 7) or with SPDA data environment 320. It is, for example, contemplated to include SPDA environment 320, computation environment 330 and analysis environment 340 within one computer environment.

The results of the analysis performed in analysis environment 340 are acquired MES environment 350, as is schematically illustrated in FIG. 7. When the analysis shows that chamber 312 and 314 do not meet a predetermined matching processing performance or processing criteria, an MES decision is made to intervene in the process. This intervention can be an automated/closed loop intervention from MES environment 350 to chambers 312 and 314 using for example links 550 and 552 which are schematically depicted on FIG. 7. Optionally, a non-automated intervention can be executed using the same links. Such intervention can include adjusting processing parameters, conducting equipment maintenance or repair of chamber 312 and/or chamber 314. Optionally, non-automated MES intervention can be executed using these links.

As schematically illustrated in FIG. 8, automated and non-automated MES intervention with chamber 312 can be executed through controllers 410, 412, 414, 416, 418 and 420, as well as information input devices 422 and 424. Typically, a wafer fab tool such as chamber 312 employs an on-board computer or distributed computer function in order to operate or control various processes and operational functions and it will be understood that MES environment 350 (FIG. 7) and SPDA data environment 320 may require special protocols in order to access chamber 312. Reporting environment 360 can acquire data and other information from the various environments of the present invention, as is schematically illustrated in FIG. 7. For example, when MES environment 350 is linked to chamber 312 through bidirectional links 550 and 552, a report can simultaneously be generated in reporting environment 360 through link 554. Reports generated by reporting environment 360 include printed matter, display on a computer monitor and voice. These reports can be generated in real time. It is also contemplated to

provide reports generated by this environment to a network such as network 516 shown in FIG. 9.

SPDA techniques of the present invention have been described in connection with a processing or performance comparison between two IC processing chambers, these techniques are equally suitable for use with one chamber. For example, two processing runs can be executed in one chamber using the same processing recipe. The SPDA delta graph resulting from the same parameters of the two processing runs can then be utilized to determine if there are significant run-to-run processing or equipment performance problems. Similarly, the chamber performance of a production run can be compared with a test run through the use of an SPDA delta graph of the production run and the test run. The SPDA data of a test run or a run which is made under standardized conditions can be stored in a database such as database 513 (FIG. 9) of novel process 300. These database data can then be used in a subsequent SPDA analysis of a production run.

Additionally, the SPDA techniques of the present invention are equally suitable for evaluating metrology data concerning in-situ product testing. For example, using the technology disclosed in U.S. Pat. No. 5,698,989 (J. Nulman, 1997) for measuring the sheet resistance of an electronically conductive film on a semiconductor susbstrate in-situ, while maintaining the substrate within the vacuum environment of the semiconductor process apparatus. The SPDA data environment of the novel IC fabricating process can collect the sheet resistance data of a test run or a run made under standardized processing conditions. Subsequently, the SPDA data environment can collect sheet resistance data of a production run using the same recipe. The data can then be processed using the SPDA techniques described in connection with graphs 518 through 542, shown in FIGS. 10 – 17, to derive one or more SPDA delta graphs of the present invention. The delta graphs can be analyzed to determine if there are significant differences between the test run and the production run thus providing a technique for improving process control and wafer yield.

Another embodiment of the present invention is shown in FIG. 18, schematically illustrating novel process 600 for IC fabricating. This process utilizes SPDA techniques of the present invention in conjunction with using such processing criteria as SPC

techniques. Process 600 includes a manufacturing environment 610, an SPC data environment 620. a computation environment 630, an analysis environment 640, an MES environment 650 and a reporting environment 660. Optionally, the MES environment can also include an MIS component (not shown).

Manufacturing environment 610 of novel process 600 includes a chamber 612 (FIG. 18) for IC processing, similar to chamber 312 described in connection with FIG. 8. SPC data environment 620 collects SPC data from chamber 612, similar to the techniques described in connection with SPDA data acquisition in SPDA environment 320 of novel process 300 shown in FIG. 7. The SPC data can then be utilized to, for example, develop control charts.

SPC methodologies suitable for the present invention include control chart methodologies and Pareto charts. A Pareto chart is a bar chart representation which displays a ranking of the number of occurrences of a particular defect as compared with the cumulative number of occurrences of all defects and the number of occurrences of each of the other defects or problems. Control charts are particularly suitable for techniques of the present invention. As is well known to those of ordinary skill in the art, control limits are typically determined following the collection of a statistically significant number of data, which are relevant to an important or critical parameter indicative of the process operating as designed and resulting in an acceptable yield. A suitable parameter for a process carried out in manufacturing environment 610 can include sputter power in a sputter deposition process, gas flow rate and/or pressure, and particle contamination in the chamber environment. Metrology data measuring these parameters at specific intervals provide the input for the determination of control limits. Additionally, metrology data concerning in-situ product testing can be used in a similar way. For example using the technology disclosed in the '989 patent for measuring the sheet resistance of an electrically conductive film on a semiconductor substrate in-situ, while maintaining the substrate within the vacuum environment of the semiconductor process apparatus. The data which are obtained from the process while running in control, i.e. within operational specification and/or yield, are then computed to determine the process control limits using statistical methods which are well known to those of ordinary skill in the art. Subsequent

production runs are then analyzed using metrology data of the same processing or in-situ product parameters as were used to determine the control limits.

The SPC data in SPC data environment 620 are communicated to computation environment 630, which processes the SPC data to determine the control limits for the process which was executed in chamber 612. These data processing techniques are well known to those of ordinary skill in the art. SPC data regarding production runs in chamber 612 are then collected in SPC environment 620, using the same recipe as was used to determine the control limits, and evaluating the same processing parameter or chamber metrology. These production run data are processed in computation environment 630 to provide control charts, using methods and techniques which are well known to those of ordinary skill in the art. Computation environment 630 is employed to provide a synchronized graph overlay of two of these control charts. The graph overlay is then processed in computation environment 630 to provide a delta graphs, using techniques similar to those employed for the preparation of delta graphs 536, 540 and 542 shown in FIGS. 14, 16 and 17. Subsequently, the delta graph is analyzed in analysis environment 640 to determine if there are significant processing or performance differences between the two production runs. The result of the analysis is communicated to MES environment 650 to decide on a course of action, if any, for process intervention of chamber 612 based on the presence or absence of significant processing or performance differences between the two production runs. The SPDA technique of the present invention wherein SPDA is employed in conjunction with SPC is thus suitable for identifying and evaluating processing and/or performance differences between production runs in a processing chamber, thereby enhancing wafer yield and providing a more optimal usage of processing materials and equipment. Reporting environment 660 (FIG. 18) is adapted for generating reports from the environments of novel process 600, similar to the reports described in connection with reporting environment 360 of novel process 300.

In another embodiment of the present invention, SPDA techniques are employed for novel SPC methodologies wherein control charts are based on delta graphs as follows. A delta graph for example resulting from a performance comparison of two chambers, such as chamber 312 and 314 (FIG. 7), may indicate that there are significant performance

differences between these two chambers as illustrated in delta graphs 536, 540 and 542 shown in FIGS. 14, 16 and 17 respectively. Each of these delta graphs differs from the substantially straight line which would have resulted if there had been no significant performance differences between chambers 312 and 314 for the parameters which were tested, i.e. bias forward power, chamber pressure and RF peak-to-peak voltage. The novel SPC methodologies of the present embodiment are provided to determine process or product control limits and to optionally provide an automated process intervention technique if these limits indicate that the process is operated outside the control limits.

An SPC delta graph control chart according to the present invention is prepared by collecting a statistically significant number of delta charts for a specific comparison for example between two processing chambers, between two processing runs in the same chamber, or between two lots of semiconductor structures fabricated in the same wafer fab tools. The delta graphs which are obtained from the process while running in control, i.e. within operation specification and/or yield, are then computed to determine the process control limits using statistical methods which are well known to those of ordinary skill in the art. For example, historical data collected from delta graphs of chamber comparisons using bias forward power differences, such as are illustrated in graph 536 shown in FIG. 14, can be used to determine the range of bias forward power differences which were observed when the chambers were known to be acceptably matched. This range can then be used to set control limits indicating a satisfactory performance match between these chambers. The delta graph of any subsequent comparison between chambers can then be evaluated to determine if the graph is within the predetermined control limits. This evaluation can be conducted visually by showing the predetermined control limits on the delta graph, or numerically by listing delta graph data compared with the relevant control data. Advantageously, this novel SPC technique can be used to provide an alarm when the process is not within the predetermined control limits using methods which are well known to those skilled in the art. Alternatively, an automatic process intervention such as aborting the process run can be initiated when the process is not within its control limits for example by automatically entering the alarm signal in an MES environment such as MES environment 650 which is described in connection with FIG. 18.

It is also contemplated to provide a novel product or a novel apparatus comprising one or more digitally coded data structures including the novel SPC methodologies based on the novel delta graphs stored in a memory. Suitable memories for this novel product include removable electronic data storage devices, such as computer disks, magnetic tapes and optical disks. Suitable memories for a novel apparatus include data processing devices, such as computers, having a memory.

FIG. 19 is a schematic representation of another embodiment of the present invention showing equipment time states of a wafer fab tool, such as a processing chamber, of novel semiconductor fabrication process 700. These equipment time states include non-scheduled time 702, unscheduled downtime 704, scheduled downtime 706, engineering time 708, standby time 710 and productive time 712. The description of equipment states 702, 704, 705, 708, 710 and 712 is similar to the description of states 102 (FIG. 3), 104, 106, 108, 110 and 112 respectively. States 704, 706, 708, 710 and 712 of novel process 700 are integrated within one computer environment in order to facilitate centralized manual and automatic scheduling of various equipment functions and to provide an improved capability to respond to semiconductor processing conditions, as will be described more fully in connection with FIGS. 20 and 21. Suitable computer environments include microcomputers and computer systems employing one or more computers such as are well known to those of ordinary skill in the art. Each of the computer integrated equipment states is linked to the appropriate equipment using such linking techniques as are well known to those of ordinary skill in the art, using for example a communications standard such as SECS (SEMI equipment communications standard).

Returning to FIG. 19, total time period 714, is the total time during the period being measured, including the six equipment states 702 – 712. Non-scheduled time period 102 of total time 714 is not integrated in the computer environment. This time state includes recurring and non-recurring times, which are entered by the user. In this context an example of a recurring time state is a calendar of holidays which is entered ahead of time. Non-recurring non-scheduled time state includes for example power-off equipment

time which is entered after it has occurred. Total integrated time 716 includes off-line for maintenance 718 and on line for process 720. As illustrated in FIG. 20, off-line for maintenance time state 718 of the present invention comprises unscheduled downtime 704, scheduled downtime 706 and engineering time 708. Unscheduled downtime 704 includes equipment states for maintenance delay time 730, repair time 731, consumables/chemicals change time 732, out of specification input time 733, facilities related time 734 and preventive maintenance time 735. Scheduled downtime 706 comprises equipment states for maintenance delay time 740, production test time 741, preventive maintenance time 742, consumables/chemicals change time 743, setup time 744 and facilities related time 745. Engineering time 708 includes equipment states for process characterization time 750 and equipment evaluation time 751.

Service procedures module 755 of the present invention, see FIG. 20, is optionally linked to repair time state 731 of unscheduled downtime 704, and to preventive maintenance state 742 of scheduled downtime 706. Additionally, preventive maintenance time state 735 of unscheduled downtime 704 can optionally be linked to service procedures module 755. Novel service procedures module 755 includes information and/or data structures for repair and/or maintenance procedures of the wafer fab tool, as well as tool calibration procedures. The procedures can be invoked when the linked time state, such as states 731, 735 or 742 is activated. Optionally, these procedures can also include information regarding spare parts specifications and/or availability. It is also contemplated to adapt service procedures module 755 for use with browser or search techniques to locate and/or link key words or phrases to appropriate sections in the service module. These key words or phrases will automatically link a searcher, such as an equipment operator detecting an equipment malfunction, to the appropriate section in the module to assist in diagnostic, repair and maintenance procedures and routines. Such browser or search techniques are well known to those of ordinary skill in the art.

Data structures or procedures of novel module 755 (see FIG. 20) can be stored on a removable electronic data storage medium, such as computer floppy disks, removable computer hard disks, magnetic tapes and optical disks, to facilitate the use of the same procedures at different manufacturing locations. Alternatively, the data structure can be

stored on a non-removable electronic data storage medium, including a medium positioned at a location which is remote from the tool, using such storage devices as are well known to those of ordinary skill in the art. The data structures or procedures of module 755 can be communicated from a remote location to the tool using communication techniques which are well known to those of ordinary skill in the art including hard wire connections, wireless connections and data communication methods utilizing one or more modems or techniques using one or more computers commonly known as servers. Novel services module 755 can be operably connected to the tool using methods and device components which are well known to those of ordinary skill in the art.

As shown in FIG. 21, on line for process time state 720 comprises standby time state 710, load/unload productive time state 770 and on line for out of specification time state 780. Load/unload productivity time state 770 includes equipment states for production time 771, engineering time 772, scheduled qualification time 773 and unscheduled qualification time 774, wherein qualification time refers to the time which is used to evaluate and qualify the tool, i.e. determine that the tool is operating satisfactory, after a tool change has been made. Production time state 771 comprises equipment states for regular production time 775, rework of product time 776, production time split with engineering time 777 and production for third party time 778. On line for out of specification time state 780 (FIG. 21) has an unscheduled time state 781 which has a maintenance delay time state 782.

A user, such as a wafer fab operator or technician, of novel process 700, illustrated in FIGS. 19 – 21, has the option to change or enable a state by interacting with the computer environment of the process through for example a keyboard command, a voice command or a pointing device such as a mouse or a light pen, using methods and technologies which are well known to those of ordinary skill in the art. The main equipment states are enabled as follows. Productive time state 712 (FIG. 19) is enabled when the user of the process or a host computer commands a load/unload state 770 (FIG. 21). Standby time state 710 (FIGS. 19 and 21) is enabled by the user. The standby state will be enabled automatically following a predetermined time interval, such as five

minutes, if the user has not provided a standby input. Engineering time state 708 (FIGS. 18 and 19) provides optional user inputs to select process characterization 750 (FIG. 20) or equipment evaluation 751. Engineering time state 708 is allocated to engineering time state 772 (FIG. 21) as part of productive time state 712 (FIG. 19) if no user input is provided in time state 708.

Scheduled downtime state 706 (FIGS. 19 and 20) and associated states 740, 741, 742, 743, 744 and 745 (FIG. 20) are enabled by the user through interaction with the computer environment of the process, for example using a light pen command.

Unscheduled downtime state 704 (FIGS. 19 and 20) is enabled by a user during off-line for maintenance time state 718 when the product such as semiconductor wafers, or the fabricating process do not meet the required quality or performance criteria, using for example control charts to make this determination. Processing of the last wafer in the tool is completed and the host computer is alerted to the occurrence of a processing fault condition. Standby state 710 (FIGS. 19 and 21) is automatically enabled when the user does not provide an input or response to the unscheduled downtime state. The process remains in total integrated time state 716 (FIG. 19) unless the user provides an input corresponding to a non-scheduled time state 702.

On line for out of specification time state 780 (FIG. 21) is automatically activated when the product or process do not meet predetermined quality or performance criteria during the on line for process time state 720. State 780 automatically advances to unscheduled time state 781 which can enable an alarm condition, such as an audible or visible alarm, to alert the user to the occurrence of an out of specification event. State 781 automatically advances to maintenance delay state 782 which puts novel process 700 in a standby state. Maintenance delay state 782 requires user intervention for progressing to any other equipment time state of process novel 700. The automatic activation of time state 780 can be linked to process/quality control techniques. For example the novel SPC techniques using the SPDA techniques of the present invention can be adapted to provide an MES environment, such as MES environment 650 (FIG. 18), with an input indicating that the process is not within its control limits. This MES input can then cause novel

process 700 to automatically invoke an online for out of specification time state 780 (FIG. 21), automatically resulting in maintenance delay state 782 which means that the process is aborted at this time state.

In another embodiment of the present invention, the novel equipment time states described in connection with FIGS. 19 – 21 are adapted to keep track of, and respond to, one or more maintenance trigger events. The expression "maintenance trigger event" as defined herein, includes events which automatically enable preventive maintenance time state 742 (FIG. 20) and service procedures module 755. Examples of maintenance trigger events include a predetermined total wafer count, predetermined total RF hours and predetermined total operating hours of a tool following the most recent tool maintenance. These trigger events are typically defined by a user of the tool. When the trigger event occurs, preventive maintenance time state 742 is automatically enabled thereby resulting in aborting the process run. It is also contemplated to integrate a trigger event alert in the present embodiment. The term "trigger event alert" as defined herein, includes an alert signal, such as an alarm, which is activated at a predetermined condition, point or time in the process prior to the occurrence of the maintenance trigger event. For example, a process having a predetermined maintenance trigger event after 500 operating hours can have a trigger event alert after 425 operating hours, i.e. 75 hours prior to the maintenance trigger event which will automatically abort the process run.

It is also contemplated to provide a novel product or a novel apparatus comprising one or more digitally coded data structures including the novel equipment time states of the present invention such as states 704, 706, 708, 710 and 712 (Fig. 19) of novel process 700 stored in a memory. These time state data structures are adapted for communicating with an apparatus such as a wafer fab tool using for example a communications standard such as SECS. Suitable memories for this novel product include removable electronic data storage devices, such as computer disks, magnetic tapes and optical disks. Suitable memories for a novel apparatus include data processing devices, such as computers, having a memory.

The computer integrated equipment time states of novel process 700 enable a user to determine the time state of any of the linked pieces of equipment in real time and it reduces the potential for ambiguity in equipment states such as can occur where these states are not integrated in a computer environment. Novel process 700 facilitates remote equipment time state determinations or reporting in real time when novel process 700 is linked to a network, such as an LAN, using such communication techniques as are well known to those of ordinary skill in the art.

The computer integrated equipment time states of the present invention are suitable for tracking, evaluating and communicating RAM equipment performance, such as RAM equipment performance. For example, operational uptime (%) = on line process time 720 (FIG. 21) x 100%, divided by total integrated time 716 (FIG. 19), while operational utilization (%) = load/unload productive time 770 (FIG. 21) x 100%, divided by total time 714 (FIG. 19).

It will be understood that the present invention which is exemplified by novel process 700 illustrated in FIGS. 19 –21 is equally operable for processes or systems utilizing computer integrated equipment time states which differ from those described in connection with process 700.

The invention has been described in terms of the preferred embodiment. One skilled in the art will recognize that it would be possible to construct the elements of the present invention from a variety of means and to modify the placement of components in a variety of ways. While the embodiments of the invention have been described in detail and shown in the accompanying drawings, it will be evident that various further modifications are possible without departing from the scope of the invention as set forth in the following claims.

CLAIMS

I claim:

1. A method of analyzing data employing a computer, the method comprising:
   a) preparing a first graph of first data versus second data;
   b) preparing a second graph of third data versus second data;
   c) overlaying the first graph on the second graph such that the first and second graphs are synchronized; and
   d) forming a delta graph of the first and second graphs.

2. The method of claim 1 wherein overlaying comprises:
   a) identifying a shared event on the first graph;
   b) identifying the shared event on the second graph; and
   c) overlaying the first and second graphs such that the shared event of the first and second graphs coincides, whereby the first and second graphs are synchronized.

3. The method of claim 1 wherein forming a delta graph comprises subtracting data of a first of the first and second graphs, from data of a second of the first and second graphs.

4. The method of claim 1 wherein the first and third data comprise data selected from the group consisting of semiconductor processing data, semiconductor processing parameters and semiconductor metrology data.

5. The method of claim 4 wherein the second data comprises time increments.

6. The method of claim 1 wherein the first and third data comprise semiconductor processing control chart data.

7. The method of claim 1 wherein preparing a first graph comprises preparing a first graph of a first semiconductor processing tool which is operating a semiconductor process and wherein preparing a second graph comprises preparing a second graph of a second semiconductor processing tool which is operating the semiconductor process.

8. A computer implemented method of determining performance differences between semiconductor processing tools, the method comprising:
   a) executing a processing technique in a first tool;
   b) acquiring first performance data versus time of the processing technique executed in the first tool;
   c) preparing a first graph including the first performance data versus time;
   d) executing the processing technique in a second tool; and
   e) overlaying the first graph on the second graph such that the first and second graphs are synchronized; and
   f) forming a delta graph of the first and second graphs.

9. A computer implemented method of determining control limits of a processing technique, the method comprising:
   a) executing the processing technique on n occurrences;
   b) determining criteria indicating satisfactory performance of the processing technique;
   c) determining m occurrences of the n occurrences wherein the processing technique meets the criteria;
   d) constructing a delta graph of each of the m occurrences; and
   e) deriving control limits from the delta graphs of the m occurrences.

10. The method of claim 9 wherein n comprises a statistically significant number.

11. A method of controlling a process, the method comprising:
   a) executing the process;
   b) generating process data;

c) preparing a first graph of first data versus second data;

d) preparing a second graph of third data versus second data;

e) forming a delta graph of the first and second graphs;

f) analyzing the delta graph, thereby obtaining analysis results;

g) comparing the analysis results with predetermined process criteria; and

h) adjusting the process if the results do not meet the criteria.

12. The method of claim 11, wherein the method is implemented by a computer.

13. The method of claim 11, wherein the process comprises a semiconductor fabrication process.

14. An apparatus comprising an environment adapted for: (1) acquiring first data versus second data, (2) acquiring third data versus second data, (3) plotting the first data versus the second data, thereby forming a first graph, (4) plotting the third data versus the second data, thereby forming a second graph and (5) constructing a delta graph of the first and second graphs.

15. The apparatus of claim 14 comprising a semiconductor processing tool.

16. An apparatus for controlling a process, the apparatus comprising:

a) a first environment adapted for: (1) acquiring first data versus second data, (2) acquiring third data versus second data, (3) plotting the first data versus the second data, thereby forming a first graph, (4) plotting the third data versus the second data, thereby forming a second graph and (5) constructing a delta graph of the first and second graphs;

b) a second environment adapted for analyzing the delta graph, thereby obtaining an analysis result; and

c) a third environment adapted for communicating the result to the process.

17. The apparatus of claim 16 additionally comprising a fourth environment adapted for: (1) comparing the analysis result with predetermined process

criteria. and (2) intervening in the process if the analysis result does not meet the process criteria.

18. The apparatus of claim 17 wherein intervening comprises automatically intervening.

19. The apparatus of claim 16 wherein the apparatus comprises a semiconductor processing tool.

20. A memory including a digitally encoded data structure adapted for forming a delta graph from a first graph and a second graph, the structure comprising:
a) a first algorithm for overlaying the first graph on the second graph. such that the first and second graphs are synchronized; and
b) a second algorithm for forming the delta graph from the synchronized first and second graphs.

21. A method for enabling an equipment time state of an apparatus, the method comprising:
a) defining equipment time states including a plurality of computer integrated time states;
b) linking each of the plurality of computer integrated time states to the apparatus; and
c) activating one of the plurality of computer integrated time states.

22. The method of claim 21 wherein activating comprises user interaction with the computer integrated time states.

23. The method of claim 21 wherein activating comprises an automatic interaction with the computer integrated time state.

24. The method of claim 21 wherein the plurality of computer integrated time states comprises one or more time states selected from the group consisting of an off-line for maintenance time state and an on-line for process time state.

25. The method of claim 21 additionally comprising accessing a service procedures module which is integrated with at least one of the plurality of activated equipment time state.

26. The method of claim 25 wherein the service procedures module comprises information selected from the group consisting of apparatus repair information, apparatus maintenance procedures and apparatus calibration procedures.

27. The method of claim 26 wherein the information is browser searchable.

28. The method of claim 21 wherein the apparatus comprises a semiconductor fabrication tool.

29. A method for enabling an equipment time state of an apparatus for executing a process wherein the process is integrated with the equipment time state, the method comprising:

a) defining equipment time states having a plurality of computer integrated time states including one or more time states which are integrated with the process; and

b) activating the one or more process integrated time states.

30. The method of claim 29 additionally comprising determining a process control limit.

31. The method of claim 30 wherein activating comprises an automated response if the process is executed outside of the control limit.

32. The method of claim 30 wherein the control limit comprises an SPC limit.

33. The method of claim 29 wherein the process comprises a semiconductor fabrication process.

34. A method for enabling an equipment time state of an apparatus for executing a process wherein the process is integrated with the equipment time state, the method comprising:

a) defining equipment time states having a plurality of computer integrated time states including one or more time states which are integrated with the process;

b) determining a process control limit comprising a delta graph technique control limit; and

c) activating the one or more process integrated time states if the process is executed outside of the control limit.

35. The method of claim 34 wherein the process comprises a semiconductor fabrication process.

36. A method for enabling a preventive maintenance time state of an apparatus for executing a process, the method comprising:

a) determining a maintenance trigger event; and

b) enabling the time state upon an occurrence of the maintenance trigger event.

37. The method of claim 36 additionally comprising a trigger event alert which is activated upon an occurrence of a predetermined condition of the process.

38. An apparatus which is adapted for executing a process, the apparatus comprising computer integrated time states.

39. The apparatus of claim 38 additionally comprising a service procedures module which is integrated with one or more of the time states.

40. The apparatus of claim 38 wherein the time states comprise one or more time states selected from the group consisting of an off-line for maintenance time state and an on-line for process time state.

41. The apparatus of claim 38 wherein at least one of the time states is automatically enabled if the process is executed outside a predetermined process control limit.

42. The apparatus of claim 41 wherein the control limit comprises an SPC limit.

43. The apparatus of claim 38 comprising a preventive maintenance time state which is enabled upon an occurrence of a maintenance trigger event.

44. The apparatus of claim 38 wherein the process comprises a semiconductor fabrication process.

45. An apparatus which is adapted for executing a process, the apparatus comprising:

a) computer integrated time states;
b) a process control limit which is determined through a delta graph technique; and
c) a link between the delta graph technique and at least one of the time states wherein the link is activated if the process is executed outside the control limit.

46. The apparatus of claim 45 wherein the process comprises a semiconductor fabrication process.

47. A memory including a digitally encoded data structure, the structure comprising time state data structures which are adapted for communicating with an apparatus.

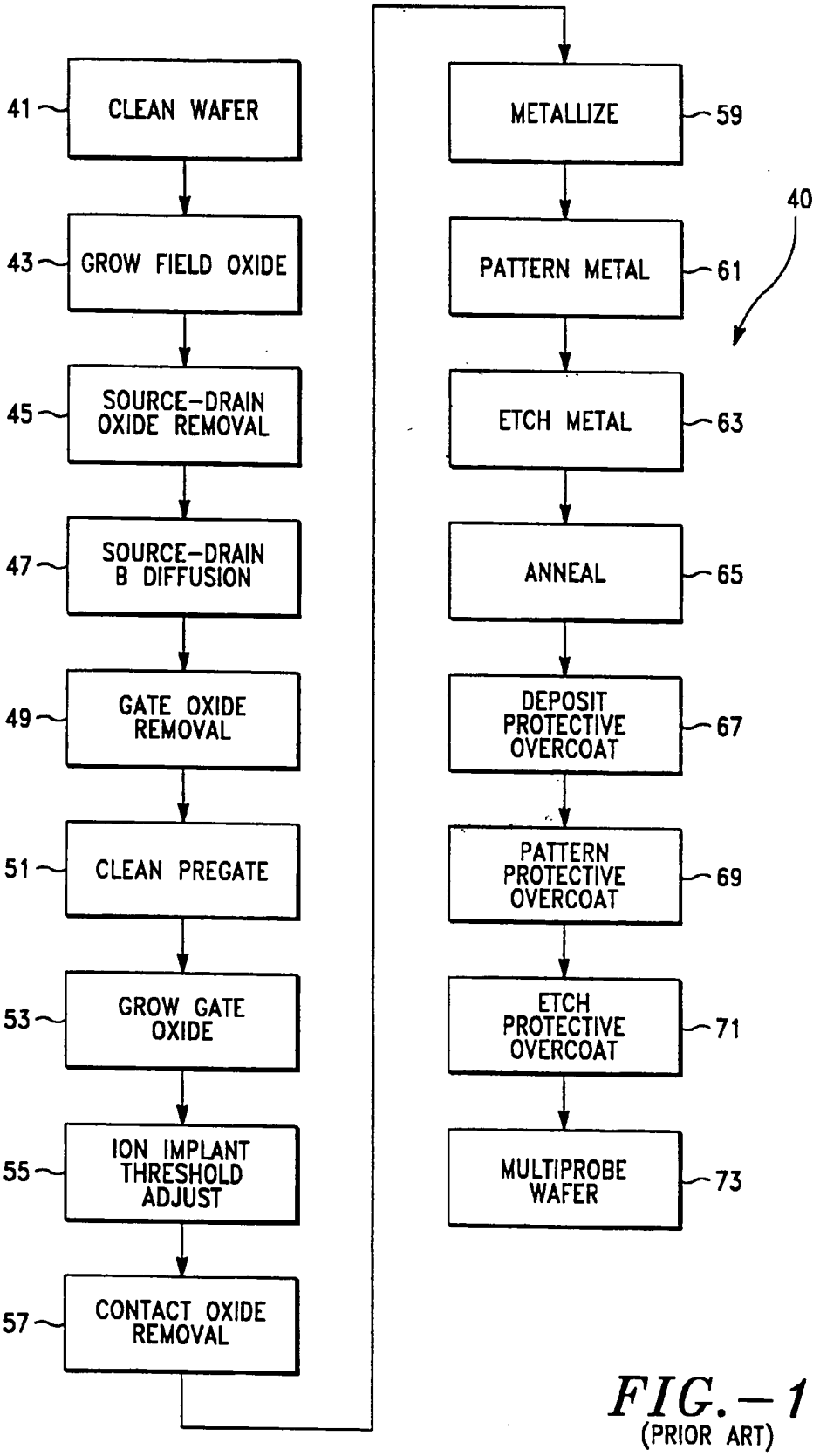

FIG.–1
(PRIOR ART)

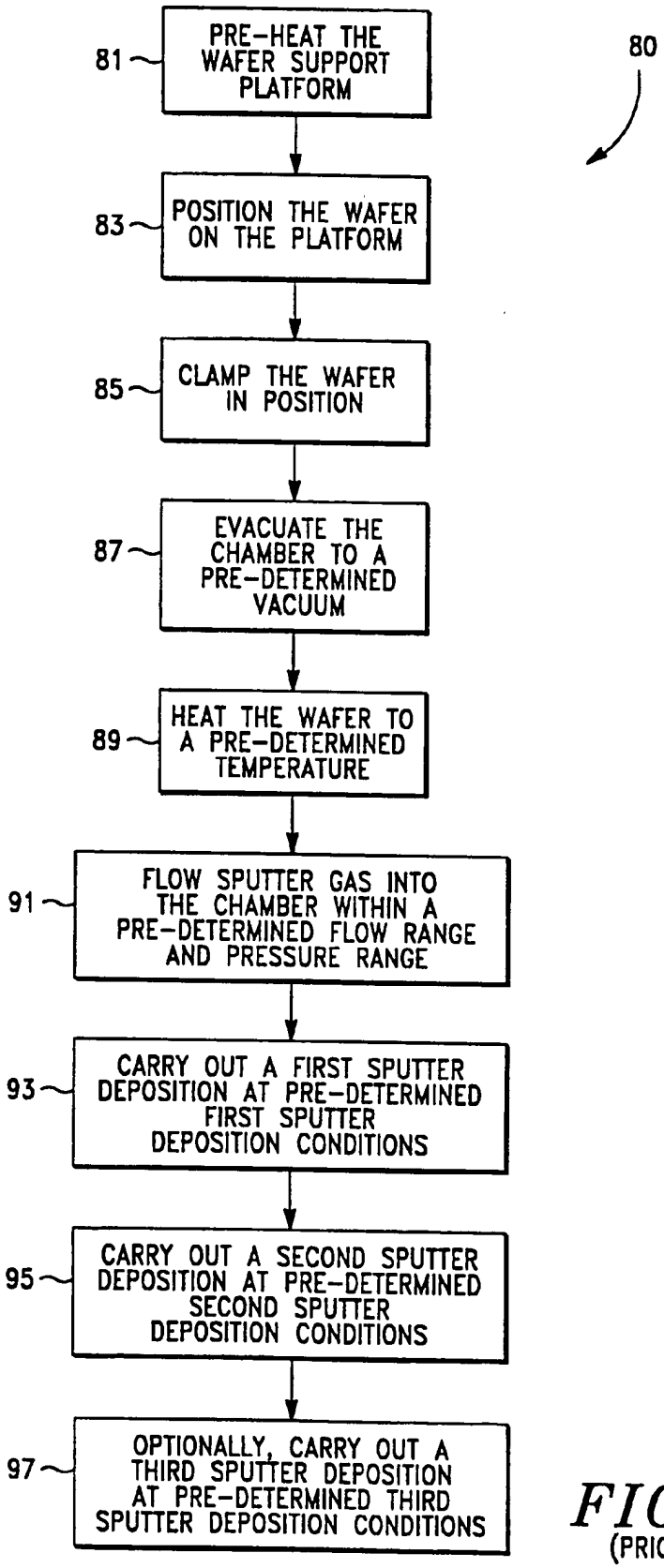

FIG.–2
(PRIOR ART)

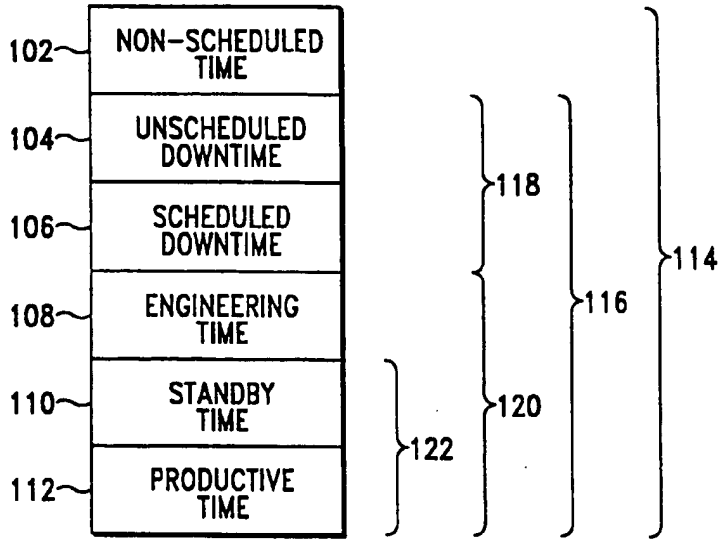

FIG.–3
(PRIOR ART)

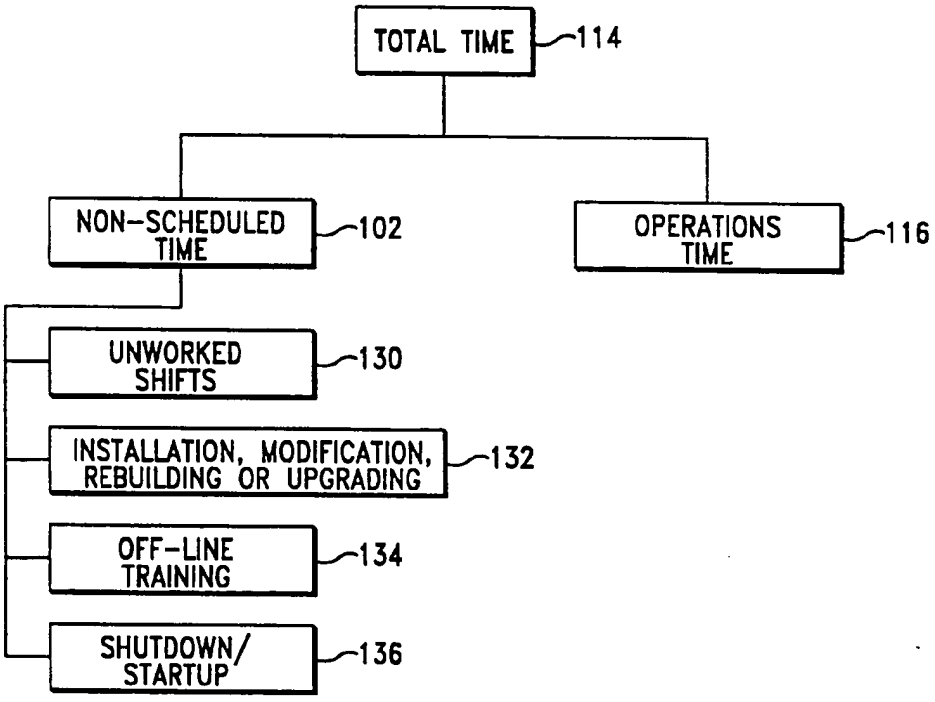

FIG.–4
(PRIOR ART)

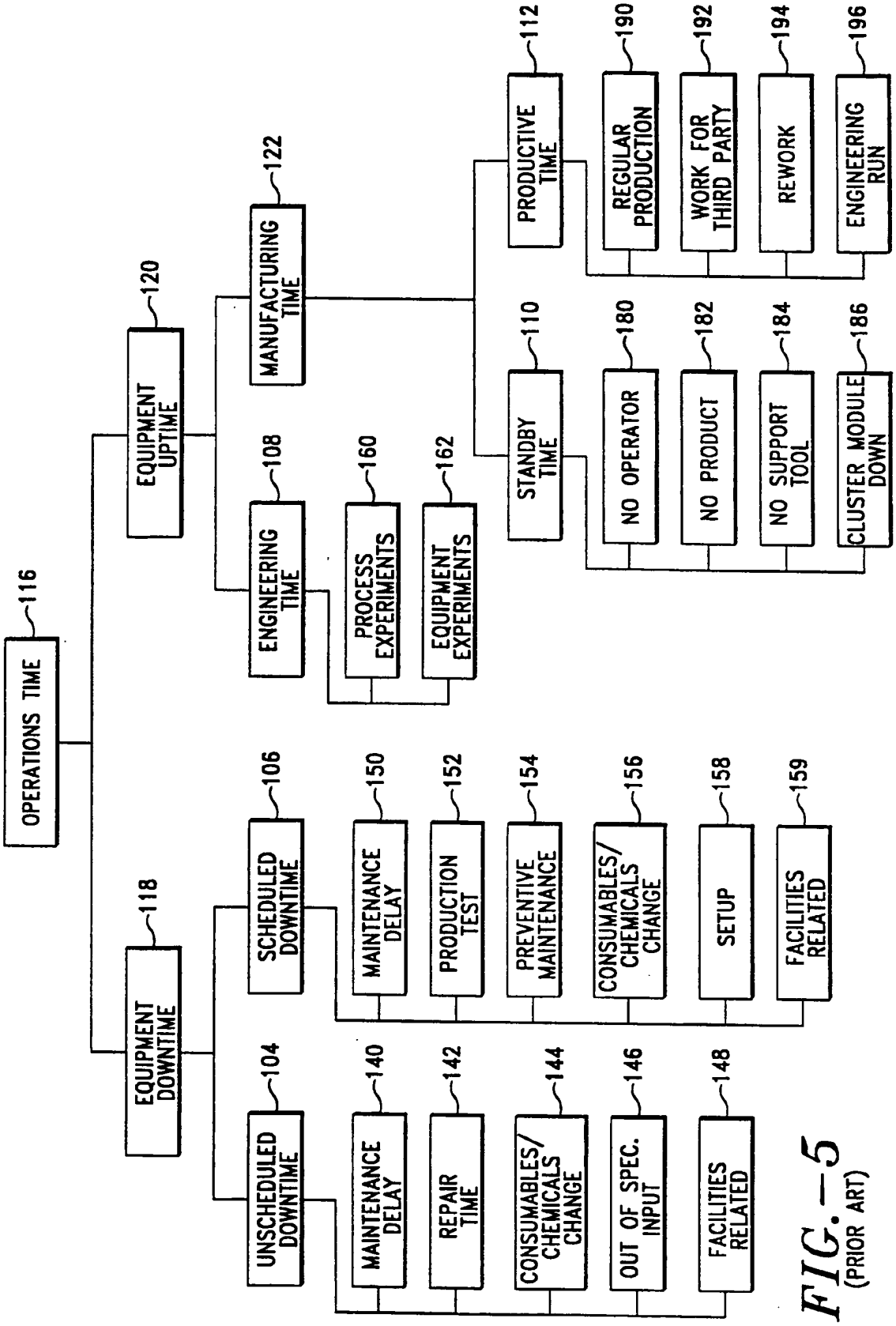

FIG.-5
(PRIOR ART)

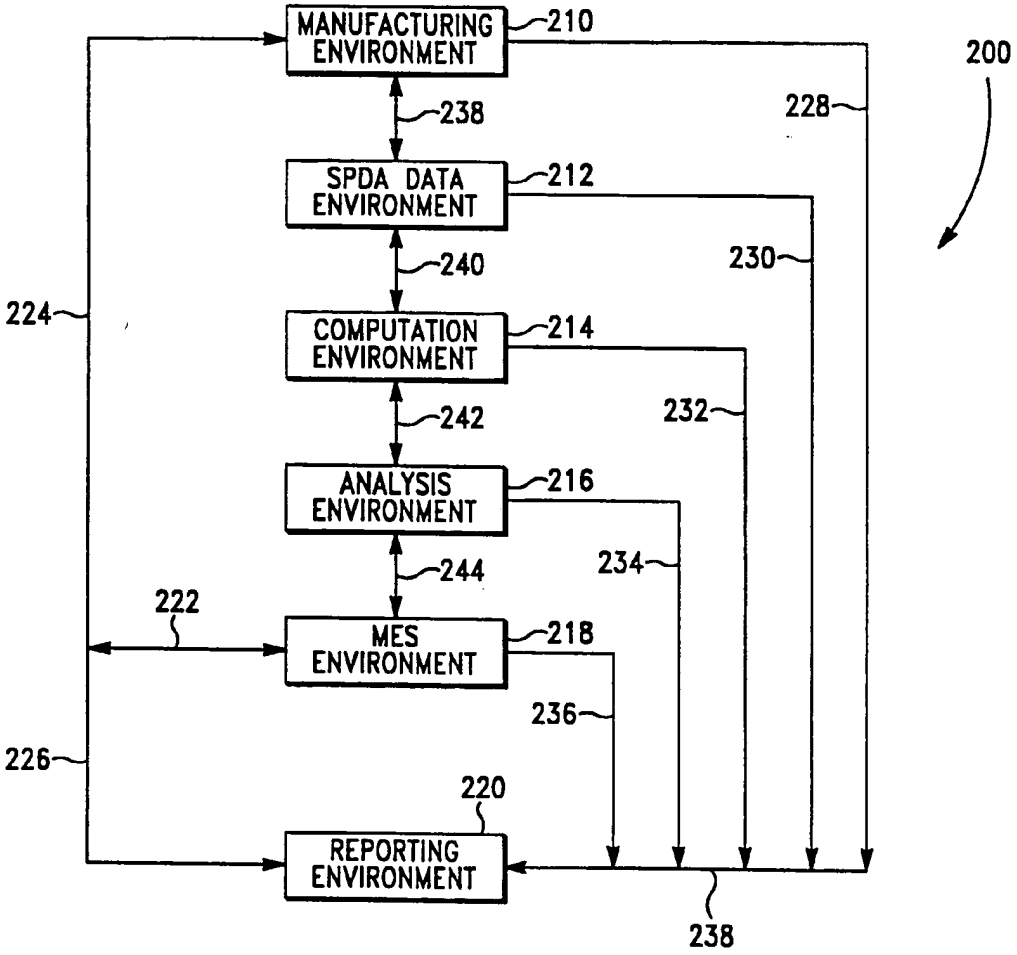
MANUFACTURING ENVIRONMENT
210
200
228
238
SPDA DATA ENVIRONMENT
212
240
230
224
COMPUTATION ENVIRONMENT
214
242
232
ANALYSIS ENVIRONMENT
216
244
234
222
MES ENVIRONMENT
218
236
226
220
REPORTING ENVIRONMENT
238

FIG.—6

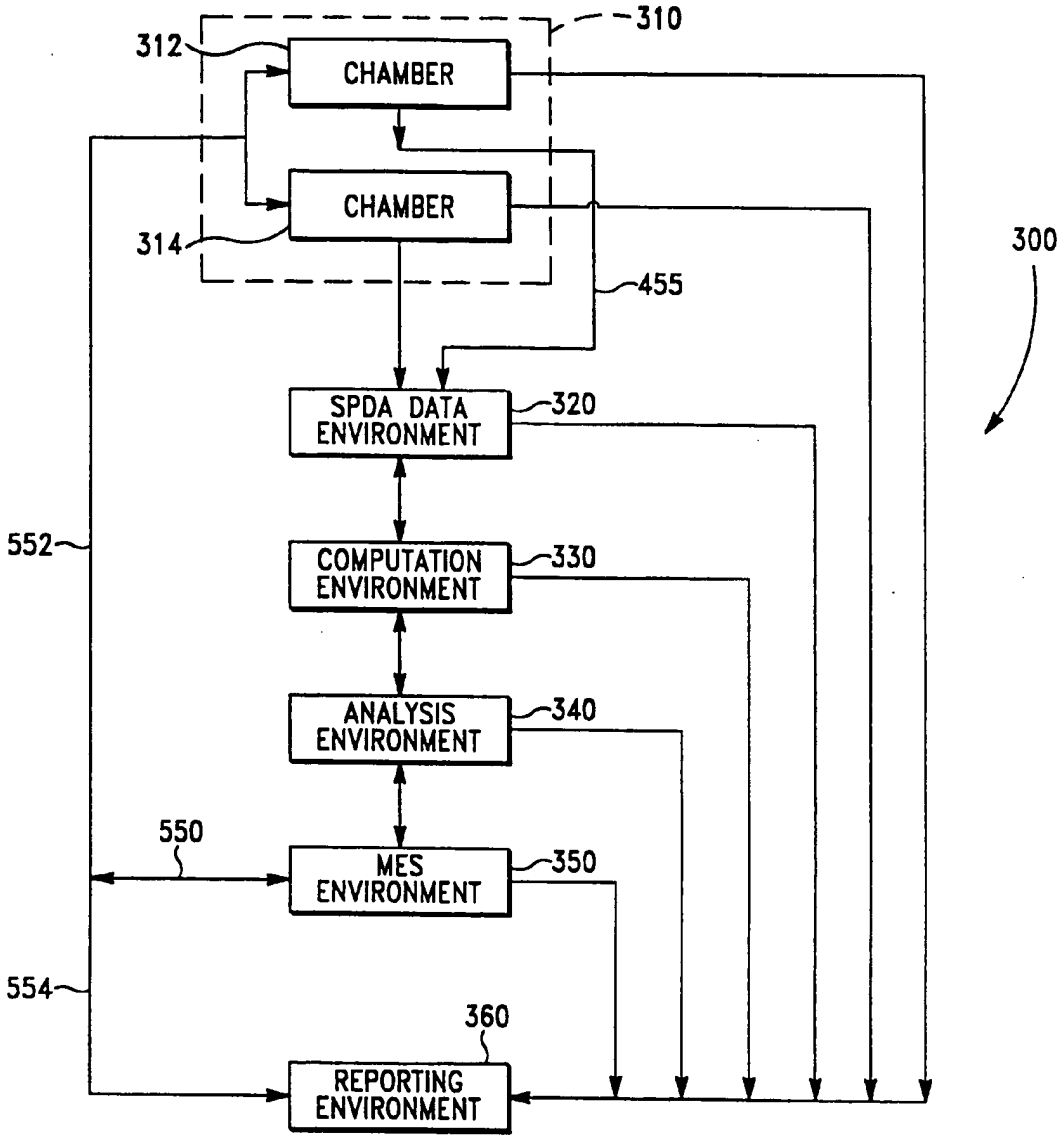
310
312
CHAMBER
CHAMBER
314
300
455
SPDA DATA ENVIRONMENT
320
552
COMPUTATION ENVIRONMENT
330
ANALYSIS ENVIRONMENT
340
550
MES ENVIRONMENT
350
554
360
REPORTING ENVIRONMENT

FIG.–7

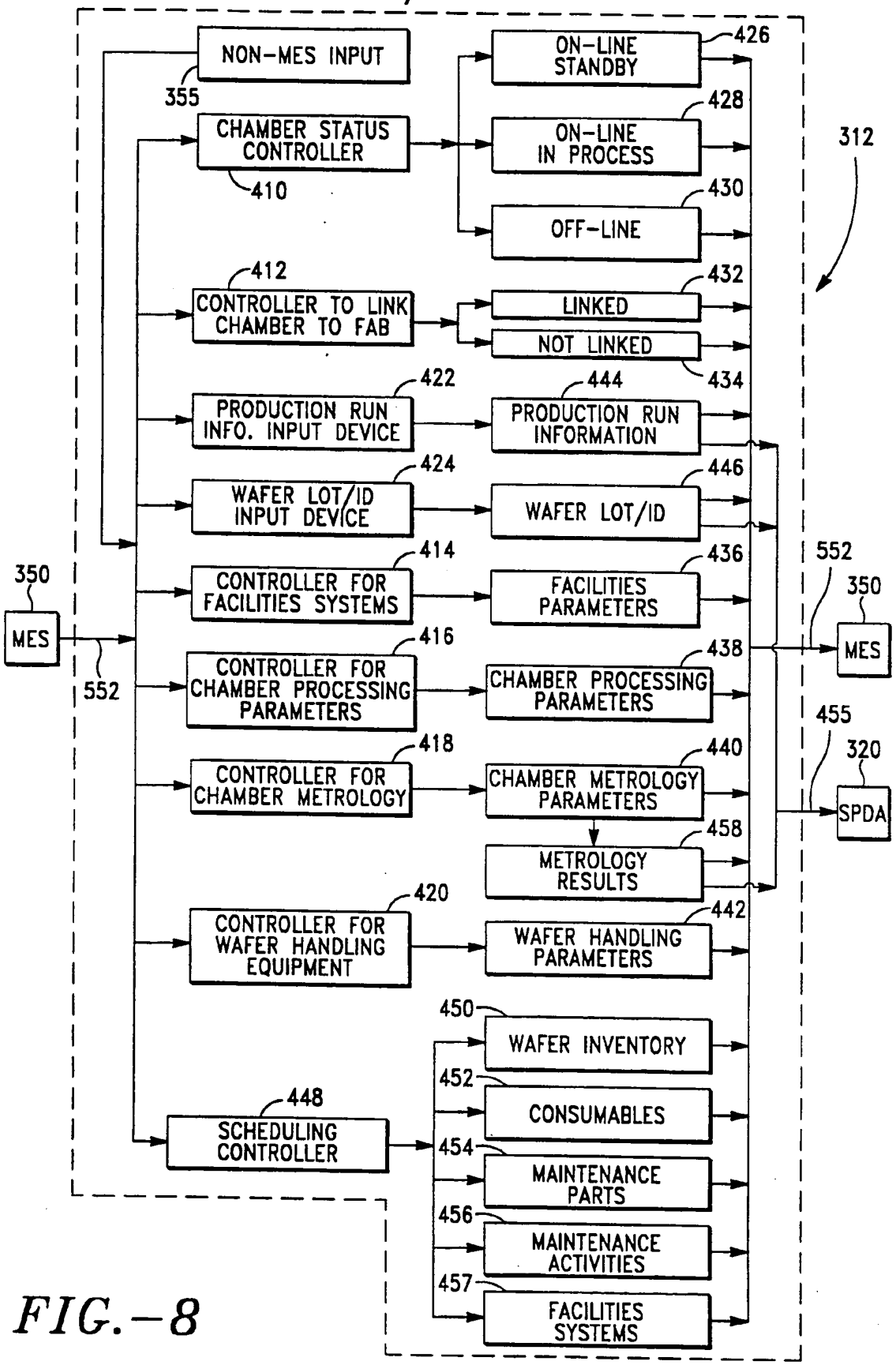
NON-MES INPUT
355
CHAMBER STATUS CONTROLLER
410
CONTROLLER TO LINK CHAMBER TO FAB
412
PRODUCTION RUN INFO. INPUT DEVICE
422
WAFER LOT/ID INPUT DEVICE
424
CONTROLLER FOR FACILITIES SYSTEMS
414
CONTROLLER FOR CHAMBER PROCESSING PARAMETERS
416
CONTROLLER FOR CHAMBER METROLOGY
418
CONTROLLER FOR WAFER HANDLING EQUIPMENT
420
SCHEDULING CONTROLLER
448
ON-LINE STANDBY
426
ON-LINE IN PROCESS
428
OFF-LINE
430
LINKED
432
NOT LINKED
434
PRODUCTION RUN INFORMATION
444
WAFER LOT/ID
446
FACILITIES PARAMETERS
436
CHAMBER PROCESSING PARAMETERS
438
CHAMBER METROLOGY PARAMETERS
440
METROLOGY RESULTS
458
WAFER HANDLING PARAMETERS
442
WAFER INVENTORY
450
CONSUMABLES
452
MAINTENANCE PARTS
454
MAINTENANCE ACTIVITIES
456
FACILITIES SYSTEMS
457
312
350
MES
552
552
350
MES
455
320
SPDA

FIG.-8

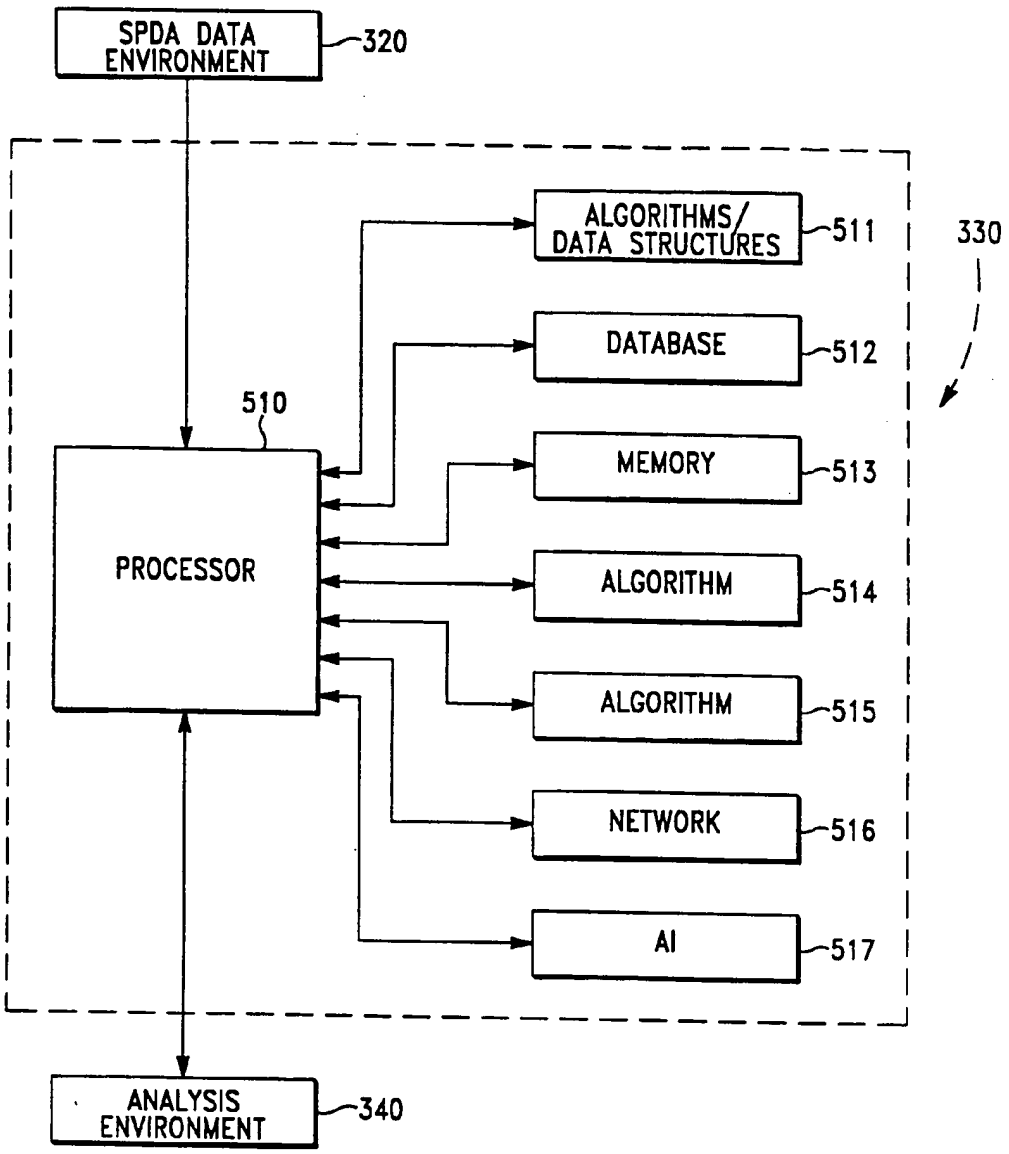
SPDA DATA ENVIRONMENT
320
330
ALGORITHMS/ DATA STRUCTURES
511
DATABASE
512
510
MEMORY
513
PROCESSOR
ALGORITHM
514
ALGORITHM
515
NETWORK
516
AI
517
ANALYSIS ENVIRONMENT
340

FIG.–9

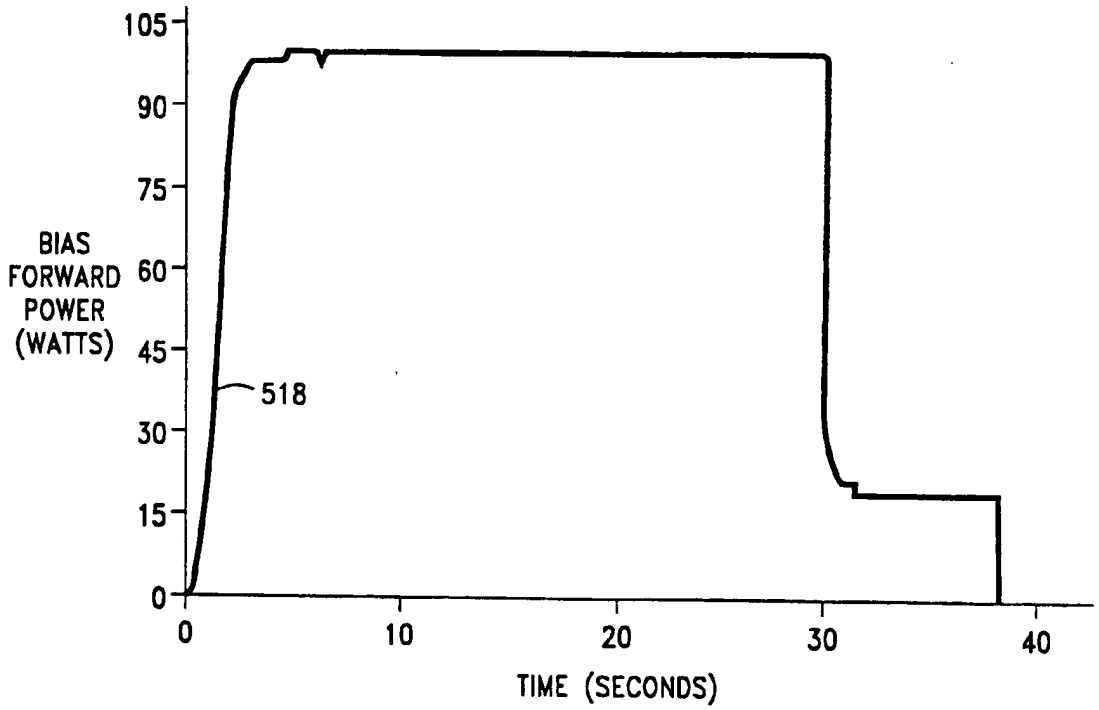
105
90
75
60
45
30
15
0
BIAS FORWARD POWER (WATTS)
518
0
10
20
30
40
TIME (SECONDS)

FIG.—10

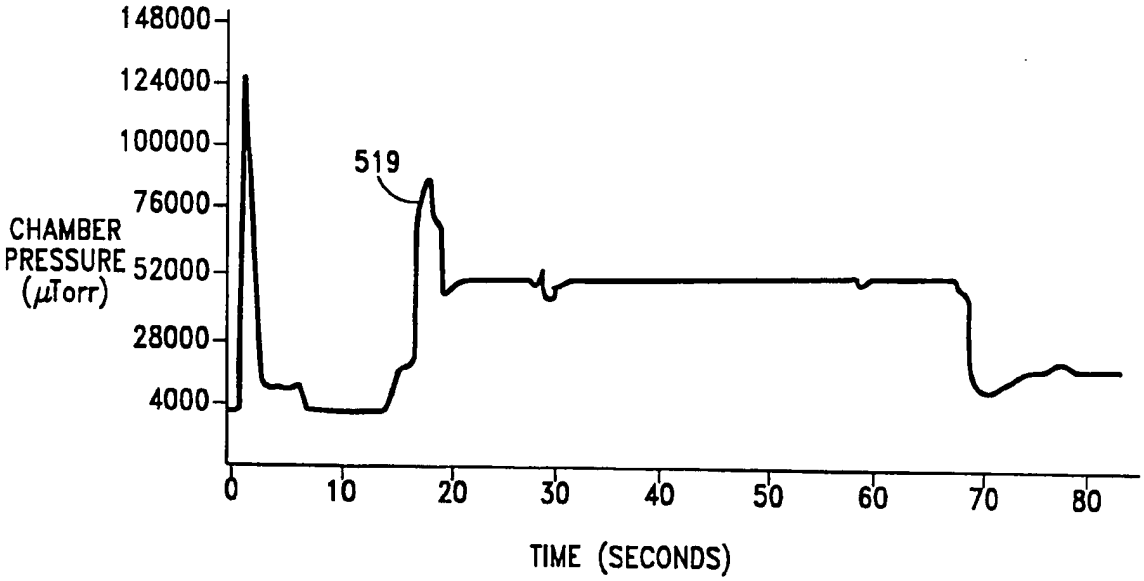
148000
124000
100000
76000
52000
28000
4000
CHAMBER PRESSURE (μTorr)
519
0
10
20
30
40
50
60
70
80
TIME (SECONDS)

FIG.—11

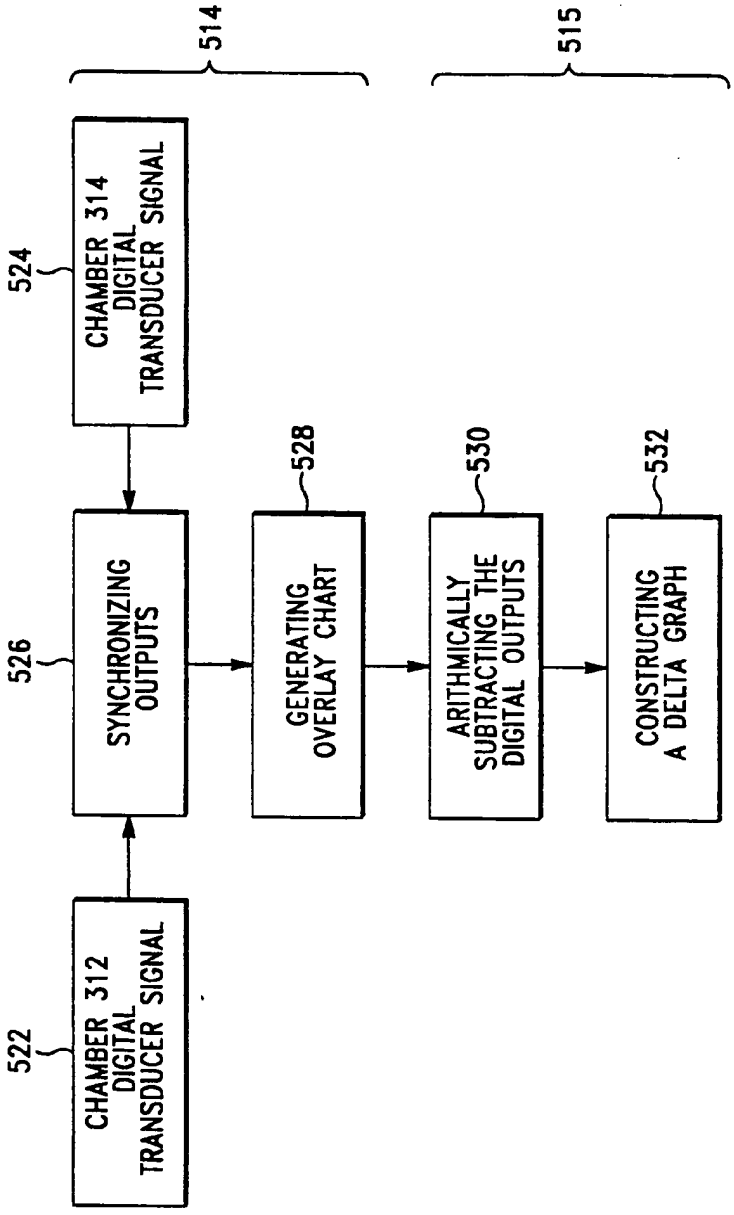
514
515
524
CHAMBER 314 DIGITAL TRANSDUCER SIGNAL
526
SYNCHRONIZING OUTPUTS
528
GENERATING OVERLAY CHART
530
ARITHMICALLY SUBTRACTING THE DIGITAL OUTPUTS
532
CONSTRUCTING A DELTA GRAPH
522
CHAMBER 312 DIGITAL TRANSDUCER SIGNAL

FIG.-12

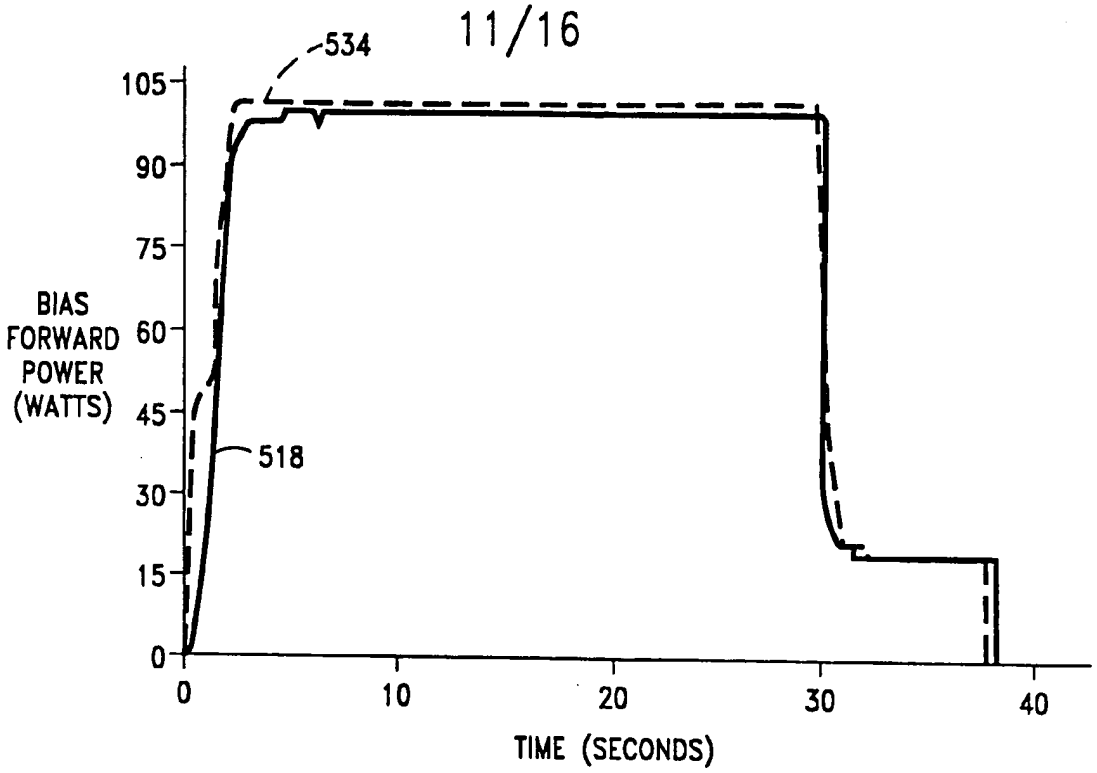
534
105
90
75
BIAS
FORWARD
POWER
(WATTS)
60
45
518
30
15
0
0
10
20
30
40
TIME (SECONDS)

FIG.—13

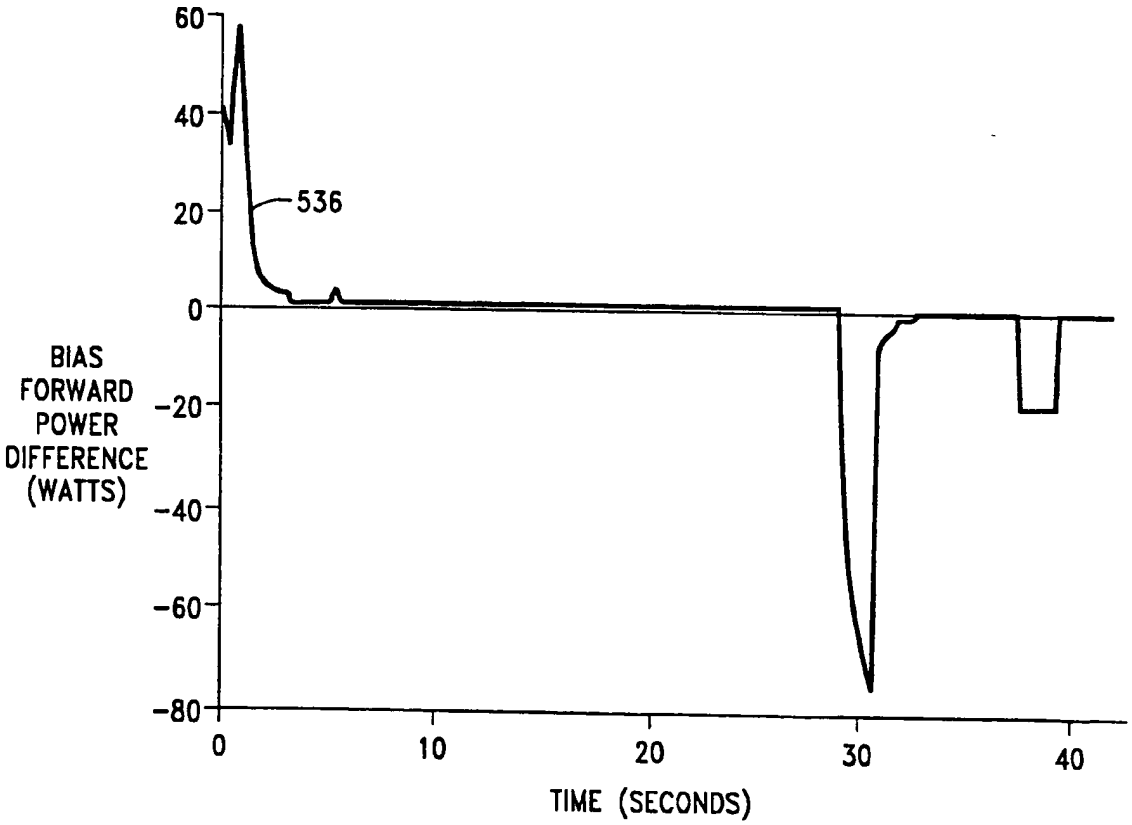
60
40
536
20
0
BIAS
FORWARD
POWER
DIFFERENCE
(WATTS)
-20
-40
-60
-80
0
10
20
30
40
TIME (SECONDS)

FIG.—14

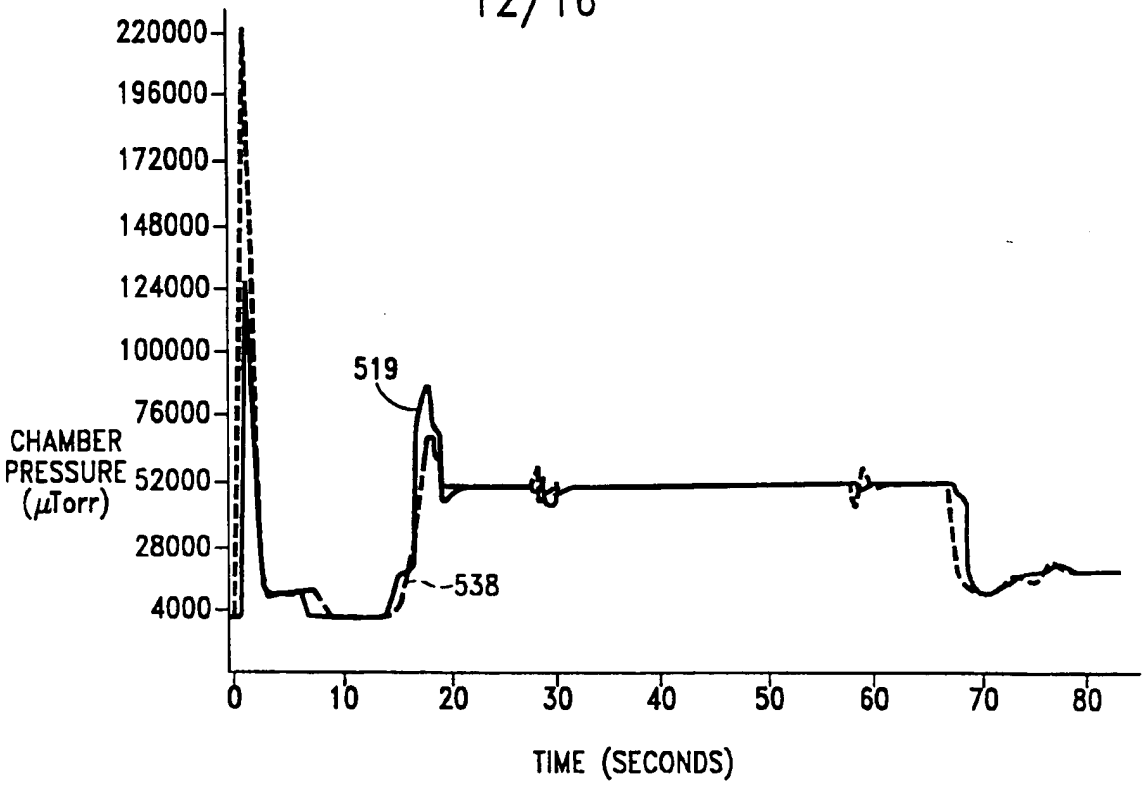
220000
196000
172000
148000
124000
100000
76000
52000
28000
4000
CHAMBER PRESSURE (μTorr)
519
538
0
10
20
30
40
50
60
70
80
TIME (SECONDS)

FIG.—15

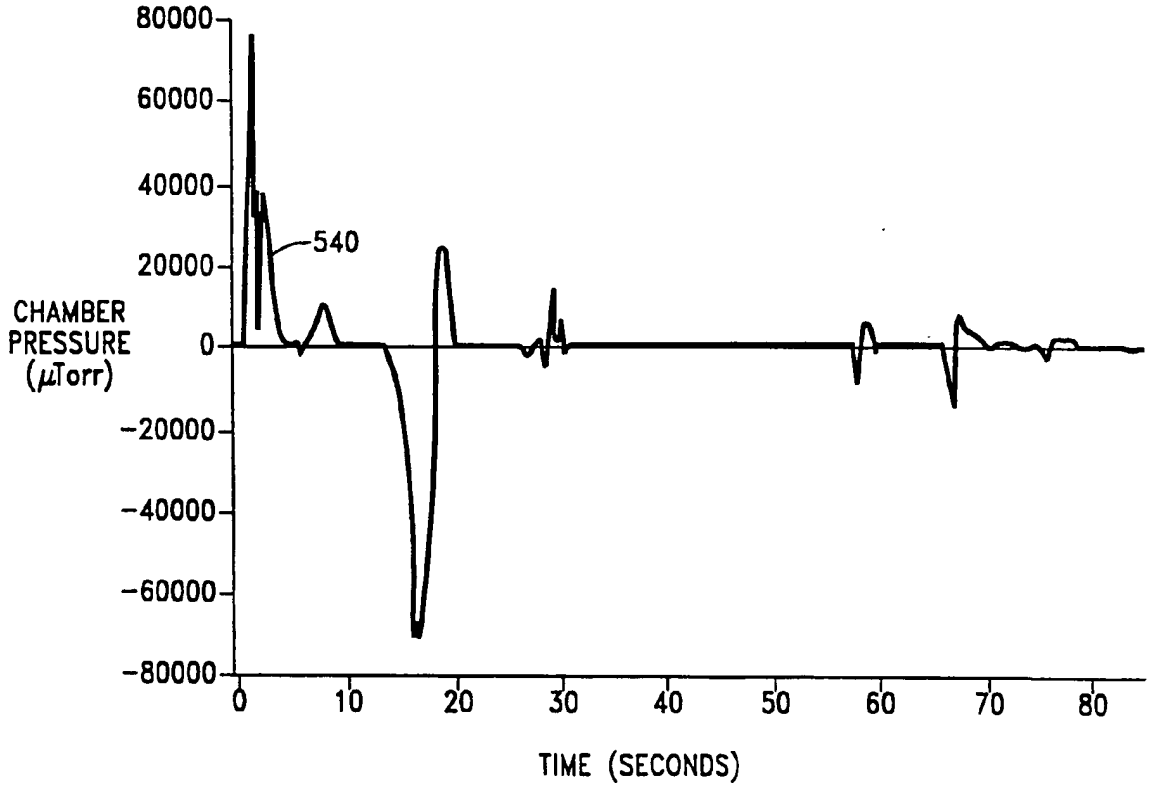
80000
60000
40000
20000
0
-20000
-40000
-60000
-80000
CHAMBER PRESSURE (μTorr)
540
0
10
20
30
40
50
60
70
80
TIME (SECONDS)

FIG.—16

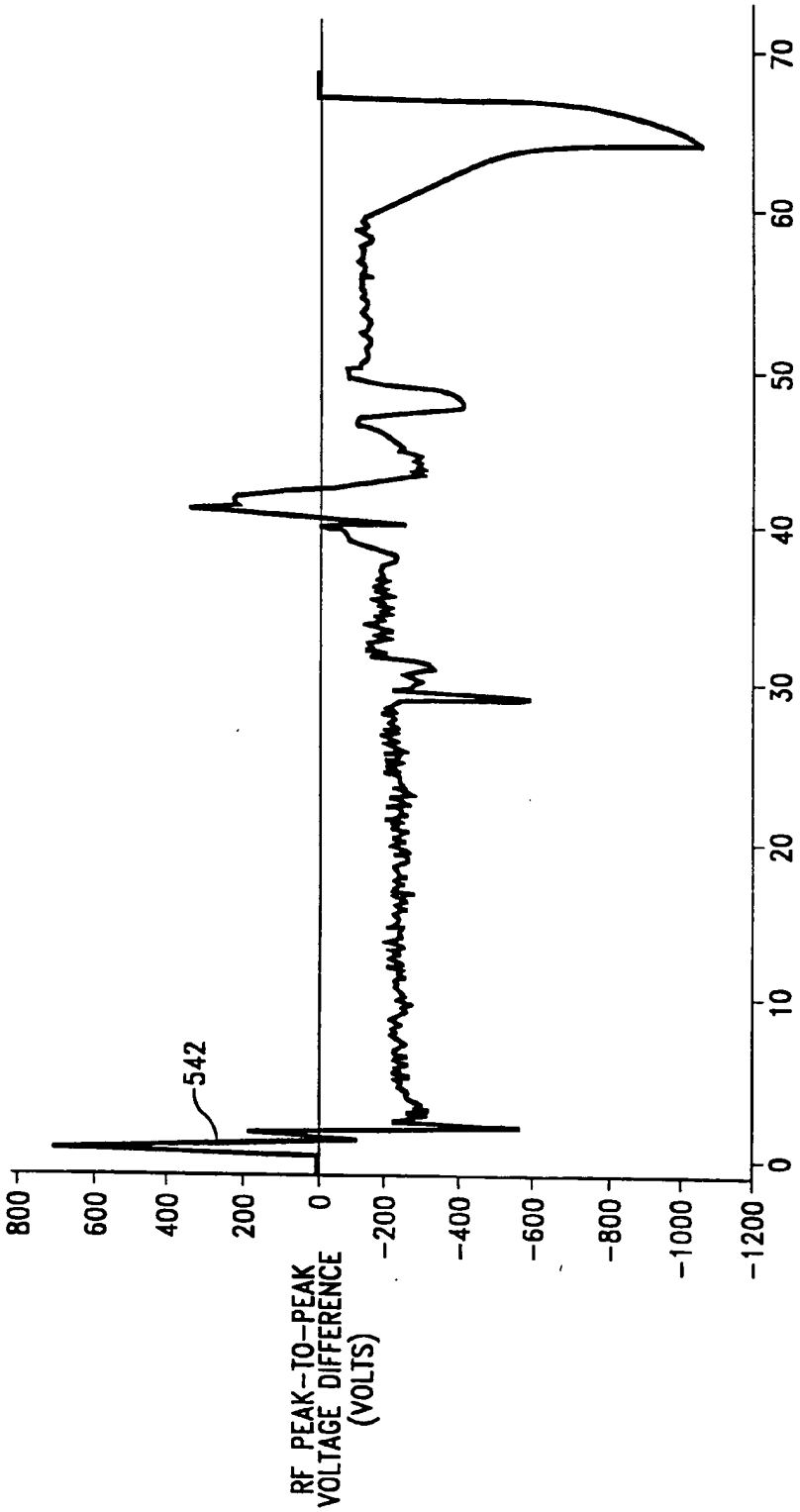
542
800
600
400
200
0
-200
-400
-600
-800
-1000
-1200
RF PEAK-TO-PEAK VOLTAGE DIFFERENCE (VOLTS)
0
10
20
30
40
50
60
70
TIME (SECONDS)

FIG.—17

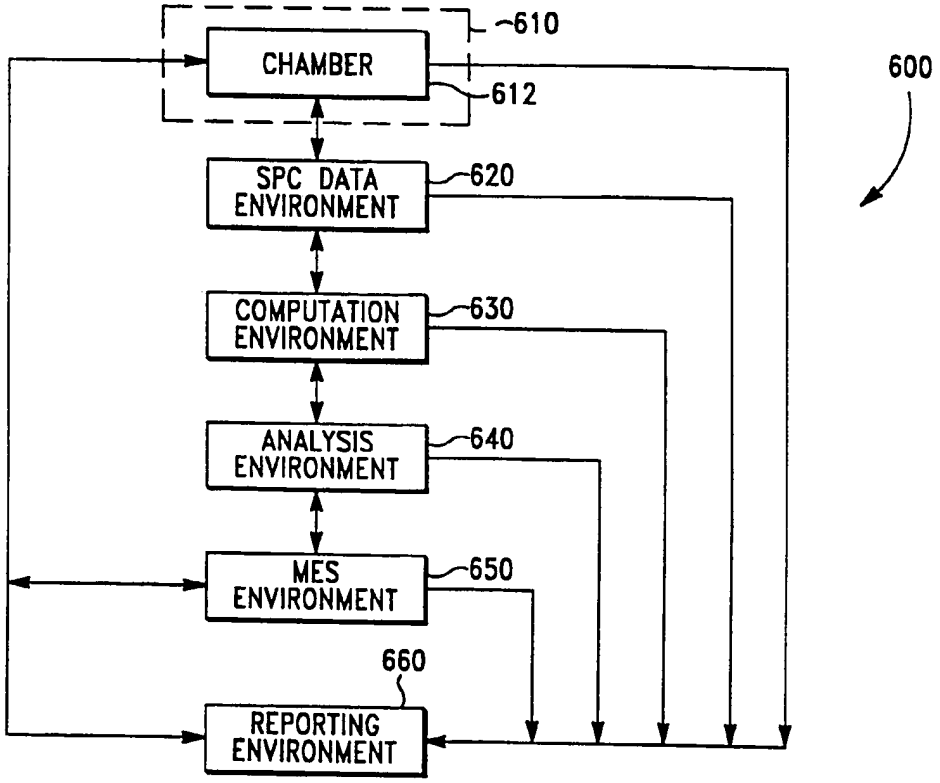
610
CHAMBER
612
600
SPC DATA ENVIRONMENT
620
COMPUTATION ENVIRONMENT
630
ANALYSIS ENVIRONMENT
640
MES ENVIRONMENT
650
660
REPORTING ENVIRONMENT

FIG.–18

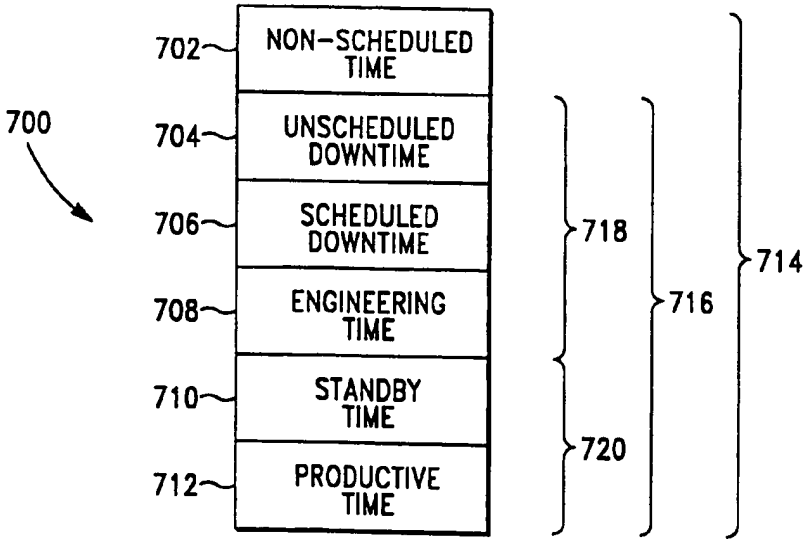
700
702
NON–SCHEDULED TIME
704
UNSCHEDULED DOWNTIME
706
SCHEDULED DOWNTIME
708
ENGINEERING TIME
710
STANDBY TIME
712
PRODUCTIVE TIME
718
720
716
714

FIG.–19

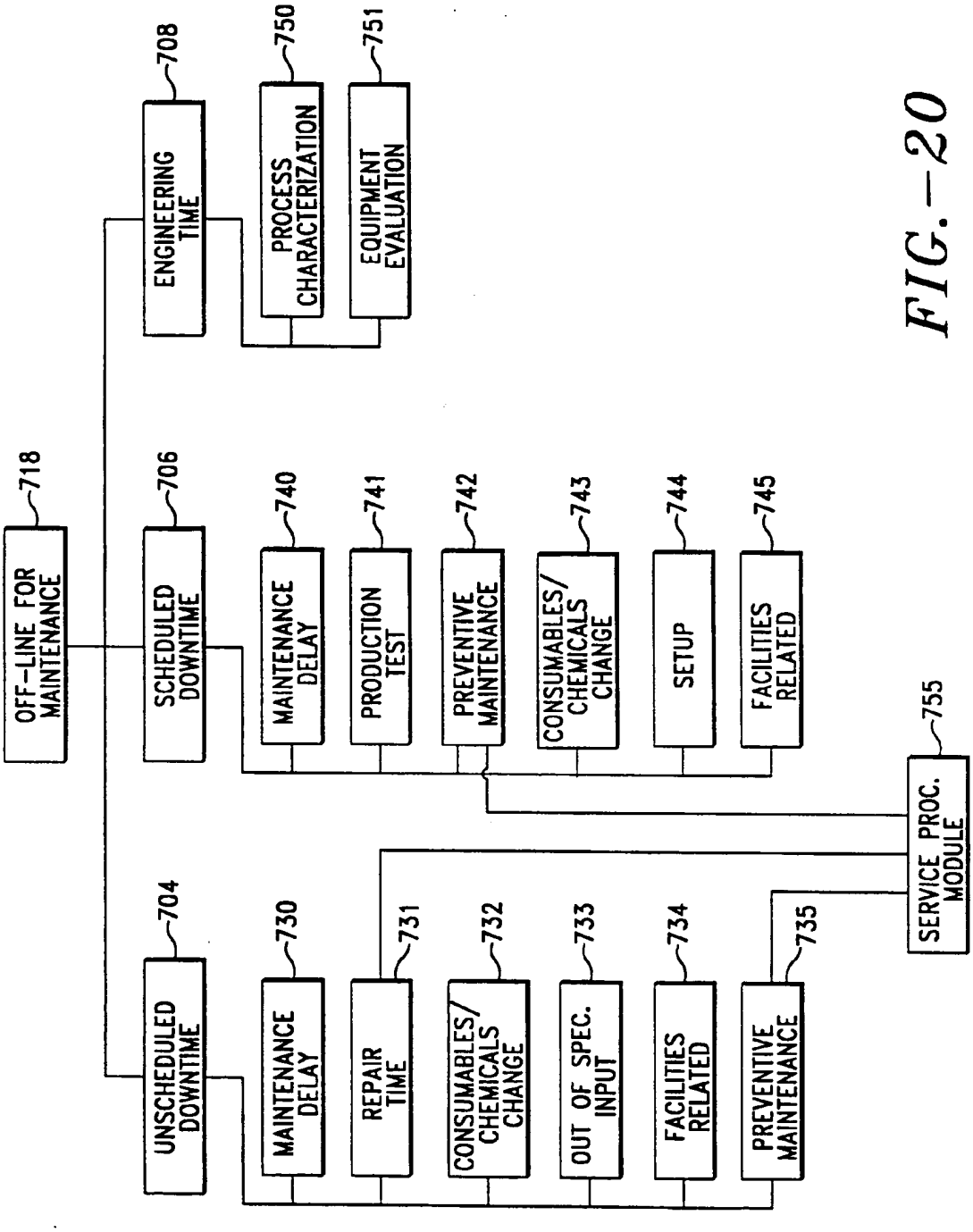
OFF-LINE FOR MAINTENANCE
718
SCHEDULED DOWNTIME
706
ENGINEERING TIME
708
MAINTENANCE DELAY
740
PRODUCTION TEST
741
PREVENTIVE MAINTENANCE
742
CONSUMABLES/ CHEMICALS CHANGE
743
SETUP
744
FACILITIES RELATED
745
PROCESS CHARACTERIZATION
750
EQUIPMENT EVALUATION
751
SERVICE PROC. MODULE
755
UNSCHEDULED DOWNTIME
704
MAINTENANCE DELAY
730
REPAIR TIME
731
CONSUMABLES/ CHEMICALS CHANGE
732
OUT OF SPEC. INPUT
733
FACILITIES RELATED
734
PREVENTIVE MAINTENANCE
735

FIG.-20

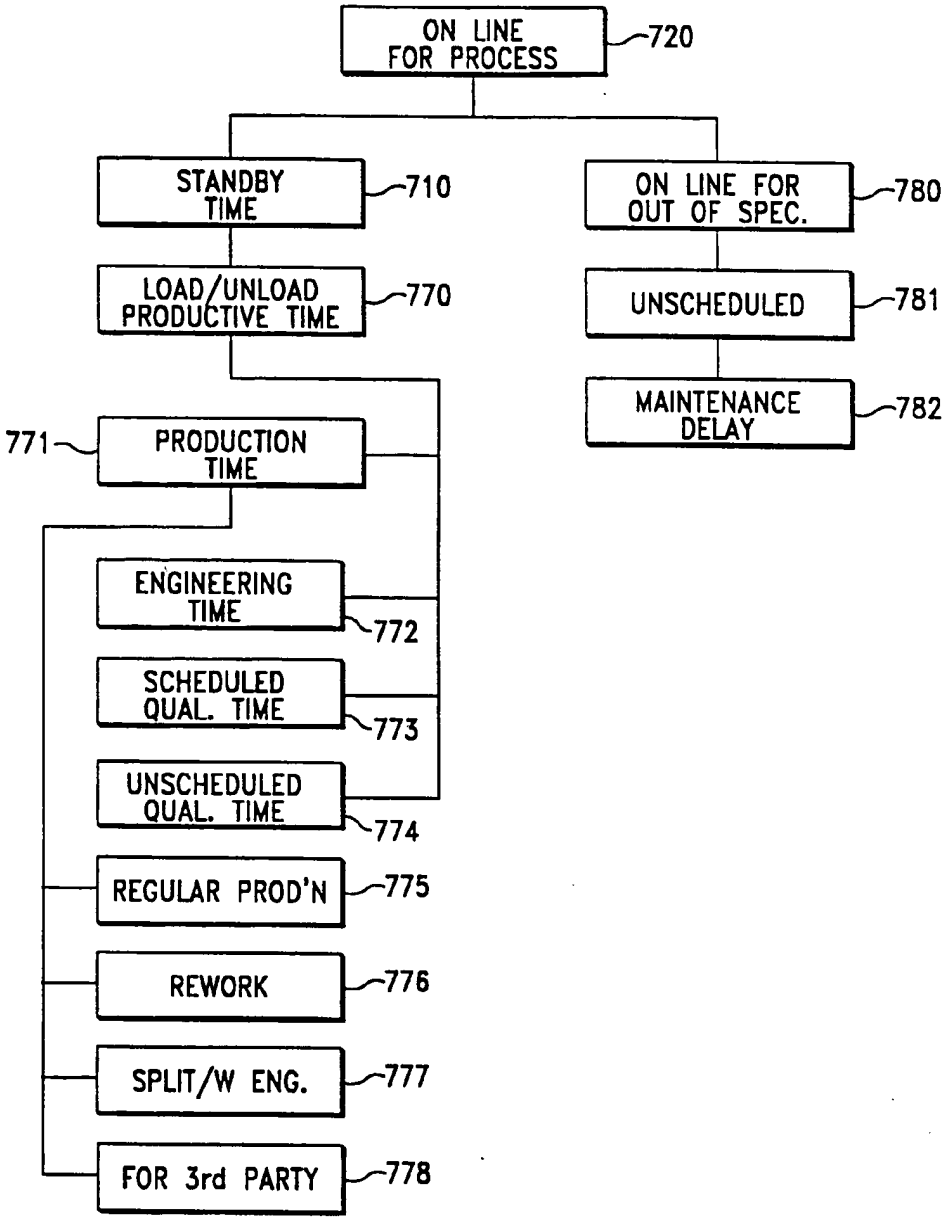
ON LINE FOR PROCESS
720
STANDBY TIME
710
ON LINE FOR OUT OF SPEC.
780
LOAD/UNLOAD PRODUCTIVE TIME
770
UNSCHEDULED
781
MAINTENANCE DELAY
782
771
PRODUCTION TIME
ENGINEERING TIME
772
SCHEDULED QUAL. TIME
773
UNSCHEDULED QUAL. TIME
774
REGULAR PROD'N
775
REWORK
776
SPLIT/W ENG.
777
FOR 3rd PARTY
778

FIG.–21

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 November 2000 (23.11.2000)

PCT

(10) International Publication Number
WO 00/70495 A3

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(22) International Filing Date: 18 May 2000 (18.05.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/314,275 18 May 1999 (18.05.1999) US

(71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventor: LYON, Richard, C.; 1224 Hopkins Gulch, Boulder Creek, CA 95006 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States (national): JP, KR, SG.

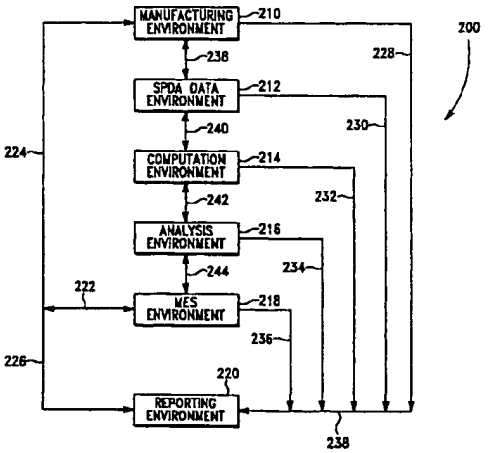
(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— With international search report.
— Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

(88) Date of publication of the international search report:
8 February 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR PROCESSING TECHNIQUES



(57) Abstract: The present invention provides a manufacturing environment (210) for a wafer fab, and an SPDA data environment (212) for acquiring processing parameters and metrology data of production runs. A computation environment (214) processes the SPDA data to prepare delta graphs (536, 540 and 542) of the present invention. These delta graphs are then analyzed in an analysis environment (216). An MES environment (218) evaluates the analysis and executes a process intervention if the results of the analysis indicate processing or product quality problems in the process run of the manufacturing environment (210). Additionally, the invention provides for SPDA delta graphs of SPC control charts as well as SPC techniques utilizing process control limits based on delta graphs to identify, analyze and trouble-shoot semiconductor processing problems, in order to improve equipment reliability and wafer yield. The present invention also provides a process (700) for computer integrated equipment time states including a service procedures module (755) linked to preventive maintenance time states (735 and 742) and to a repair time state (731).

WO 00/70495 A3

INTERNATIONAL SEARCH REPORT

In. ational Application No
PCT/US 00/13916

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G05B19/418

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 410 473 A (KANEKO MUTSUO ET AL) 25 April 1995 (1995-04-25) column 3, line 37 -column 12, line 16; figures 3-12	1-3,14, 20
X	US 5 808 303 A (BEAUDRY PIERRE ET AL) 15 September 1998 (1998-09-15) column 6, line 45-67; figures 14,15	1-4, 14-16,20
X	US 5 740 429 A (WANG QINGSU ET AL) 14 April 1998 (1998-04-14) column 5, line 39 -column 18, line 47; figures 1,2	21-26, 29, 38-40,47

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 November 2000	04 12 2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Tran-Tien, T

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

In. ıtional Application No
PCT/US 00/13916

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 06, 30 June 1997 (1997-06-30) & JP 09 034535 A (MITSUBISHI ELECTRIC CORP), 7 February 1997 (1997-02-07) abstract	36-39, 41,43,47
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 08, 30 June 1999 (1999-06-30) & JP 11 067853 A (MITSUBISHI ELECTRIC CORP), 9 March 1999 (1999-03-09) abstract	1-20
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 065 (E-0884), 6 February 1990 (1990-02-06) & JP 01 283934 A (TOKYO ELECTRON LTD), 15 November 1989 (1989-11-15) abstract	1-20
A	US 5 629 216 A (WIJARANAKULA WITAWAT ET AL) 13 May 1997 (1997-05-13) abstract	1-20
A	US 5 754 297 A (NULMAN JAIM) 19 May 1998 (1998-05-19) cited in the application abstract	1
A	US 5 108 570 A (WANG CHIEN-RHONE) 28 April 1992 (1992-04-28) cited in the application abstract	1
A	US 5 698 989 A (NULMAN JAIM) 16 December 1997 (1997-12-16) cited in the application abstract	1
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 10, 31 October 1996 (1996-10-31) & JP 08 149583 A (MITSUBISHI ELECTRIC CORP), 7 June 1996 (1996-06-07) abstract	36-47
A	US 5 260 868 A (GUPTA SUBHASH ET AL) 9 November 1993 (1993-11-09) abstract	21-47
A	US 5 408 405 A (MOZUMDER PURNENDU K ET AL) 18 April 1995 (1995-04-18) abstract	21-47

-/--

5

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INTERNATIONAL SEARCH REPORT

In. ational Application No
PCT/US 00/13916

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 877 308 A (TOKYO ELECTRON LTD) 11 November 1998 (1998-11-11) abstract ---	21-47
A	PRASAD RAMPALLI ET AL: "CEPT - A COMPUTER-AIDED MANUFACTURING APPLICATION FOR MANAGING EQUIPMENT RELIABILITY AND AVAILABILITY IN THE SEMICONDUCTOR INDUSTRY" , IEEE TRANSACTIONS ON COMPONENTS,HYBRIDS,AND MANUFACTURING TECHNOLOGY,US,IEEE INC. NEW YORK, VOL. 14, NR. 3, PAGE(S) 499-506 XP000262642 ISSN: 0148-6411 the whole document -----	21-47

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 00/13916

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. [X] As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

[X] No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-20

   Semiconductor processing techniques using delta graph analysis.

2. Claims: 21-47

   Scheduling equipment time states of a semiconductor fabrication process

INTERNATIONAL SEARCH REPORT

Information on patent family members

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